CISPA
HELMHOLTZ CENTER FOR INFORMATION SECURITY

How Secure Are Commercial RISC-V CPUs?

Lukas Gerlach, Fabian Thomas | PhD Students @ CISPA (Germany)

Meltdown

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If your computer has a vulnerable processor and runs an unpatched operating system, it is not safe to work with sensitive information without the chance of leaking the information. This applies both to personal computers as well as cloud infrastructure. Luckily, there are software patches against Meltdown.

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Spectre is harder to exploit than Meltdown, but it is also harder to mitigate. However, it is possible to prevent specific known exploits based on Spectre through software patches.

ZombieLoad Attack

Return of the Leaking Dead

Watch out! Your processor resurrects your private browsing-history and other sensitive data.

After Meltdown, Spectre, and Foreshadow, we discovered **more critical vulnerabilities** in modern processors. The ZombieLoad attack allows **stealing sensitive data and keys** while the computer recovers them.

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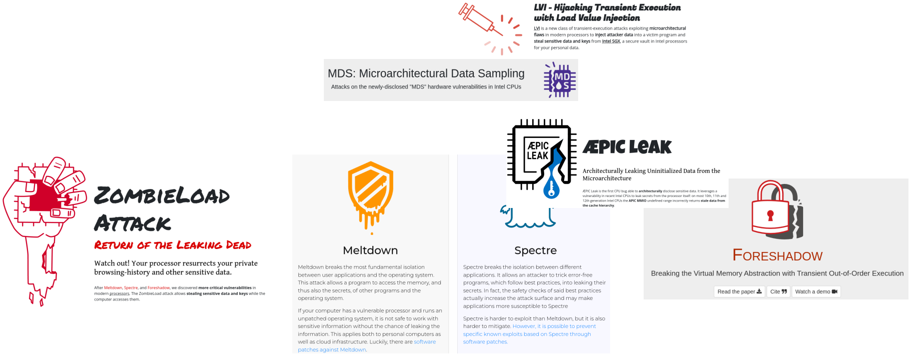
Breaking the Virtual Memory Abstraction with Transient Out-of-Order Execution

Read the paper | Cite | Watch a demo


LVI - Hijacking Transient Execution with Load Value Injection
LVI is a new class of transient-execution attacks exploiting microarchitectural flaws in modern processors to inject attacker data into a victim program and steal sensitive data and keys from Intel SGX, a secure vault in Intel processors for your personal data.
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MDS
ÆPIC LEAK
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Architecturally Leaking Uninitialized Data from the Microarchitecture
ÆPIC Leak is the first CPU bug able to architecturally disclose sensitive data. It leverages a vulnerability in recent Intel CPUs to leak secrets from the processor itself: on most 10th, 11th and 12th generation Intel CPUs the APIC MMIO undefined range incorrectly returns stale data from the cache hierarchy.
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Cross-Process Information Leak

Bulletin ID: AMD-SB-7008
Potential Impact: Information disclosure
Severity: Medium

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Under specific microarchitectural circumstances, a register in "Zen 2" CPUs may not be written to 0 correctly. This may cause data from another process and/or thread to be stored in the YMM register, which may allow an attacker to potentially access sensitive information.

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Downfall Attacks

Attack Demo FAQ Advisories Links

Downfall attacks target a critical weakness found in billions of modern processors used in personal and cloud computers. This vulnerability, identified as CVE-2022-40982, enables a user to access and steal data from other users who share the same computer. For instance, a malicious app obtained from an app store could use the Downfall attack to steal sensitive information like passwords, encryption keys, and private data such as banking details, personal emails, and messages. Similarly, in cloud computing environments, a malicious customer could exploit the Downfall vulnerability to steal data and credentials from other customers who share the same cloud computer.

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SLAP

Data Speculation Attacks via Load Address Prediction on Apple Silicon

We present SLAP, a new speculative execution attack that arises from optimizing data dependences, as opposed to control-flow dependences. More specifically, we show that Apple CPUs (implementing the ARM ISA) are equipped with a Load Address Predictor (LAP), which improves performance by guessing the next memory address the CPU will load data from based on prior memory access patterns.

FLOP

Breaking the Apple M3 CPU via False Load Output Predictions

We present FLOP, another speculative execution attack that results from recent Apple CPUs predicting the outputs of data memory accesses. More specifically, Apple M3 CPUs (4th generation and newer CPUs) are equipped with a Load Value Predictor (LVP). The LVP improves performance on data dependencies by guessing the data value that will be returned by the memory subsystem on the next access to the CPU core, before the value is actually available.

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Google researchers discover 'Reptar,' a new CPU vulnerability

November 15, 2023

Phil Venables
VP/CISO, Google Cloud

This year, Google has seen an increase in the number of vulnerabilities impacting central processing units (CPU) across hardware systems. Two of the most notable of these vulnerabilities were disclosed in August, when Google researchers discovered Downfall (CVE-2022-40982) and Zenbleed (CVE-2023-20593), affecting Intel and AMD CPUs, respectively.

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CACHE WARP

CacheWarp is a new software fault attack on AMD SEV-ES and SEV-SNP. It allows attackers to hijack control flow, break into encrypted VMs, and perform privilege escalation inside the VM.

READ | CITE | TRY

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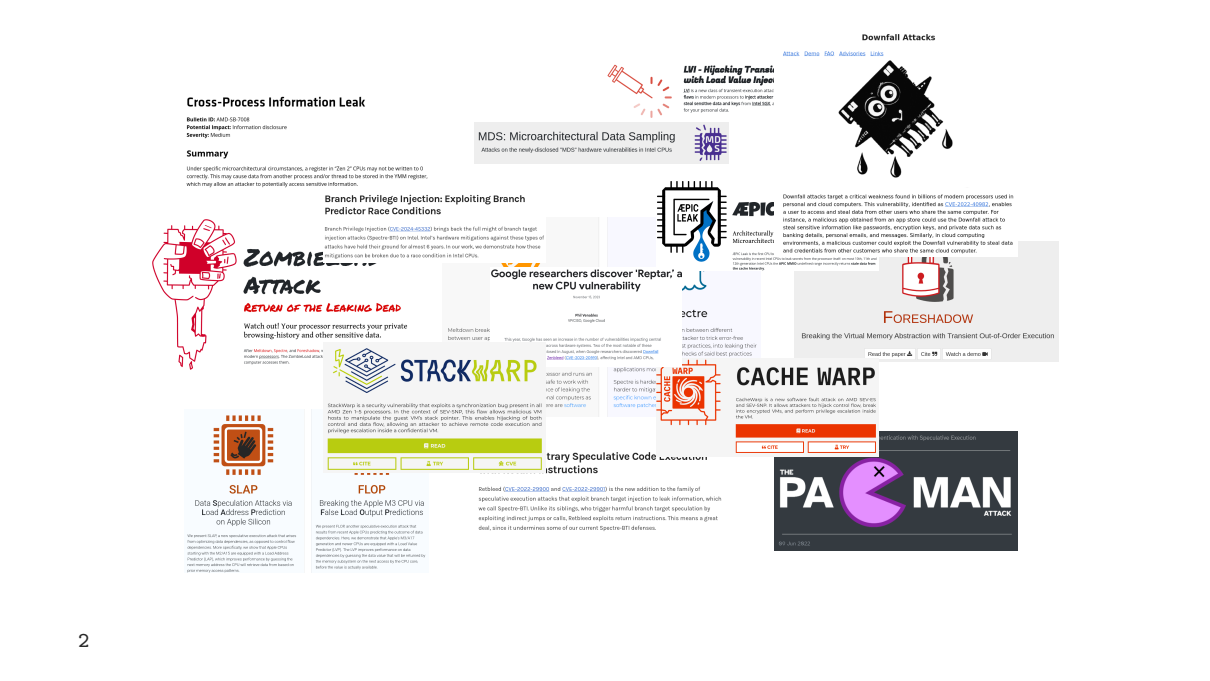
The PACMAN Attack

hentication with Speculative Execution

09 Jun 2022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Branch Privilege Injection: Exploiting Branch Predictor Race Conditions
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STACKWARP
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TRY
CVE
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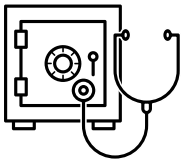
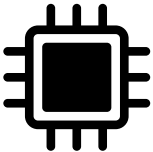
RISC-V: A Clean Slate?

Can we design a secure architecture from the start or will we repeat the same mistakes?

CPU Vulnerability Classes



Side Channels



CPU Bugs

Transient Execution

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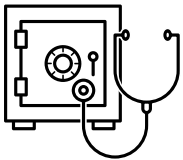

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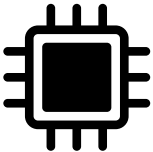

CPU Bugs

Transient Execution

Side Channels: RSA Square-and-Multiply

```
func exp_mod(C, d, n): /* M=C^d mod n */
    x = C
    for bit in d: /* MSB-first */
        x = x * x /* Square */
        if bit == 1:
            x = x * C /* Multiply */
    return x % n
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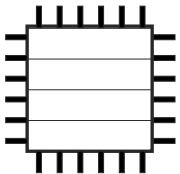
Flush+Reload

Attacker

flush

access

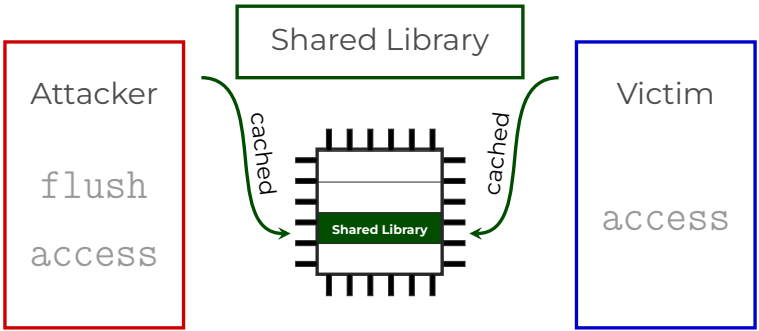
Shared Library



Victim

access

Flush+Reload



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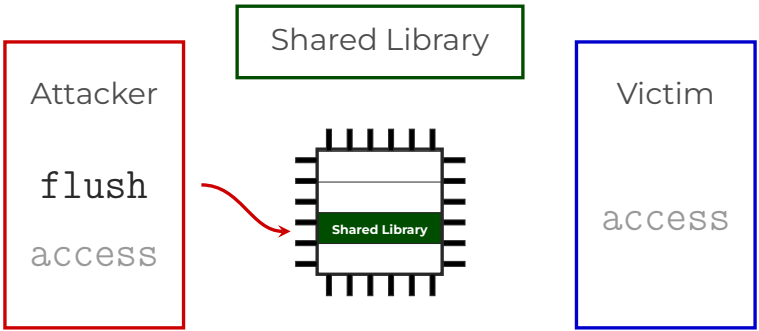

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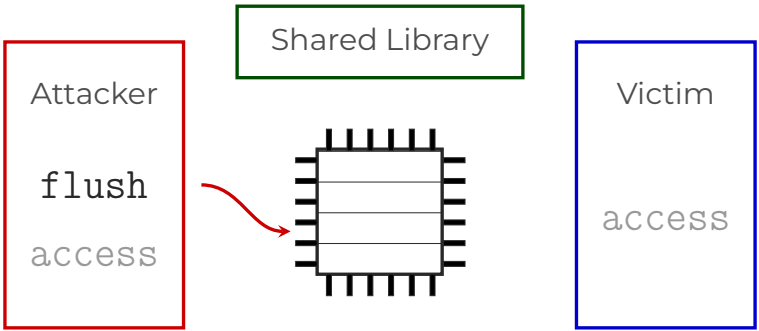

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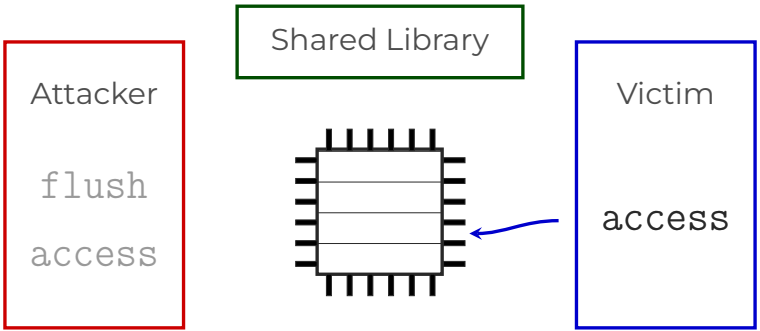

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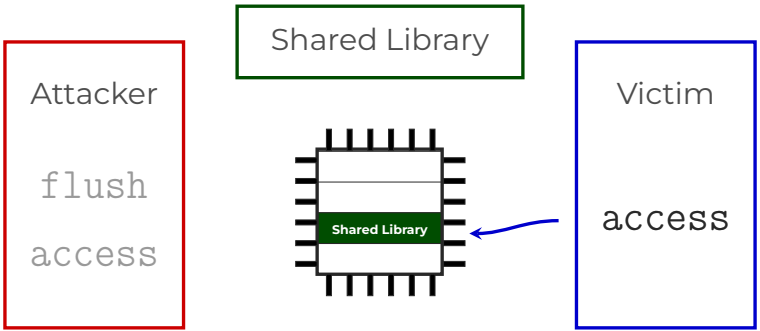

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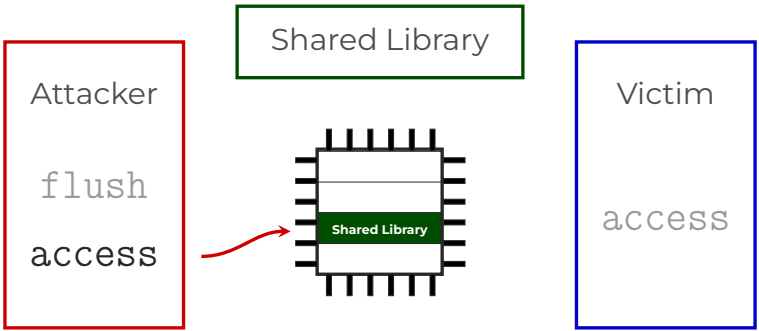

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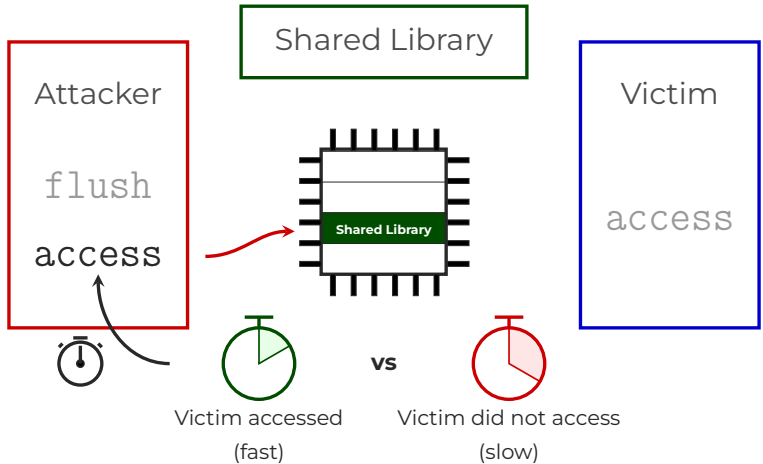

Accurate Timers?

Architectural timers

`rdcycle`	hardware cycles
`rdtime`	platform time
`rdinstret`	retired instructions

High resolution, available in user space on many cores

Cache Maintenance?

- No cache maintenance in base ISA

→ Only fences

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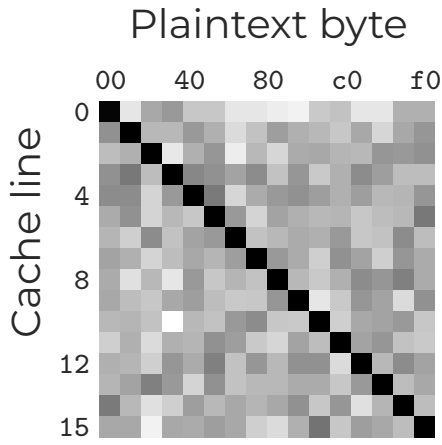
Vendor-specific cache operations

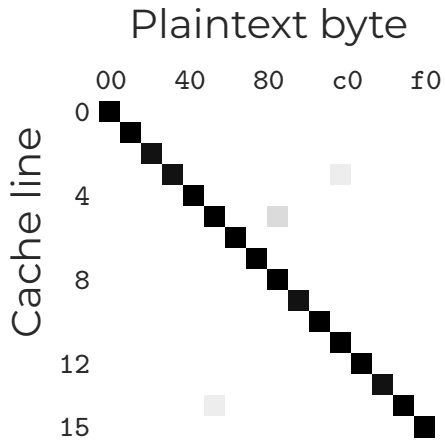
T-Head Cores:

- Unprivileged D-Cache flush by virtual address (like `clflush`)
- `fence.i` flushes entire I-Cache

AES T-Table (x86)



AES T-Table (RISC-V, C906)

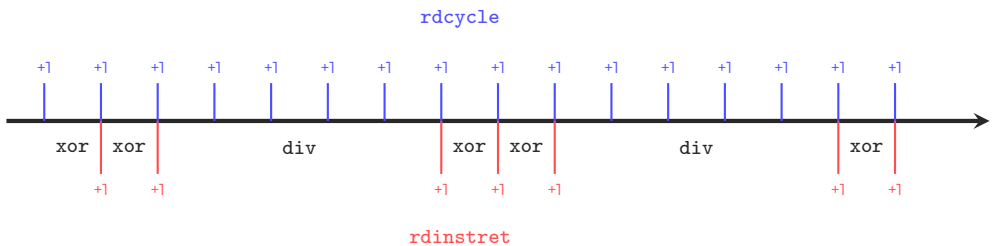


`rdcycle` **vs** `rdinstret`

CPU cycles and retired instructions can differ

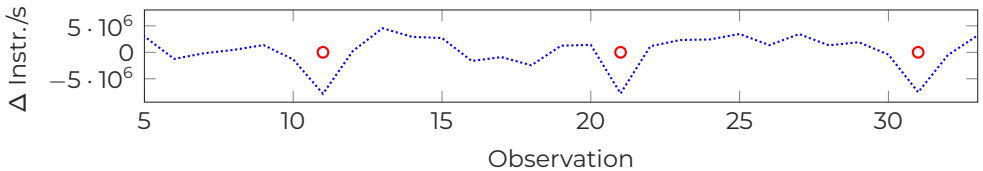
rdcycle **vs** rdinstret

CPU cycles and retired instructions can differ



CycleDrift

Drift between `rdcycle` and `rdinstret` leaks information about executed instructions (including from the kernel)



Takeaways

Accurate Timers

- ISA exposes `rdcycle`, `rdinstret` to user space
- Enables CycleDrift, precise cache timing
- ✔ Linux now disables user-space access on RISC-V

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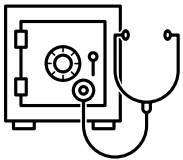
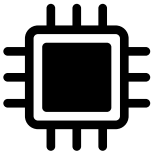
Cache Maintenance

- `fence.i` is unprivileged and flushes the entire I-Cache
- T-Head adds unprivileged D-Cache flush by virtual address (like `clflush`)
- Enables Flush+Reload on I-Cache and D-Cache.

CPU Vulnerability Classes



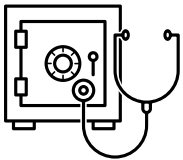
Side Channels



CPU Bugs

Transient Execution

CPU Vulnerability Classes



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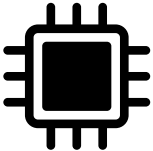

CPU Bugs

Transient Execution

Differential CPU Fuzzing

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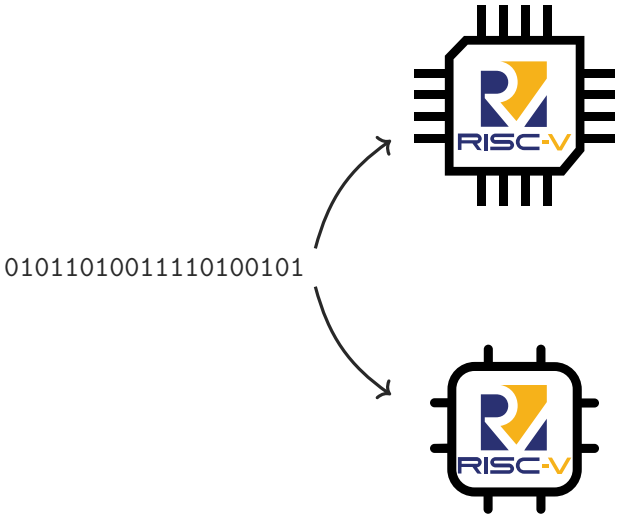

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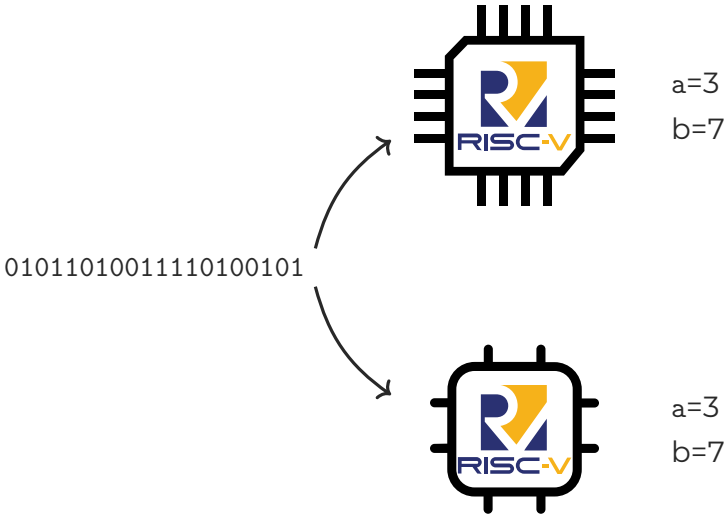

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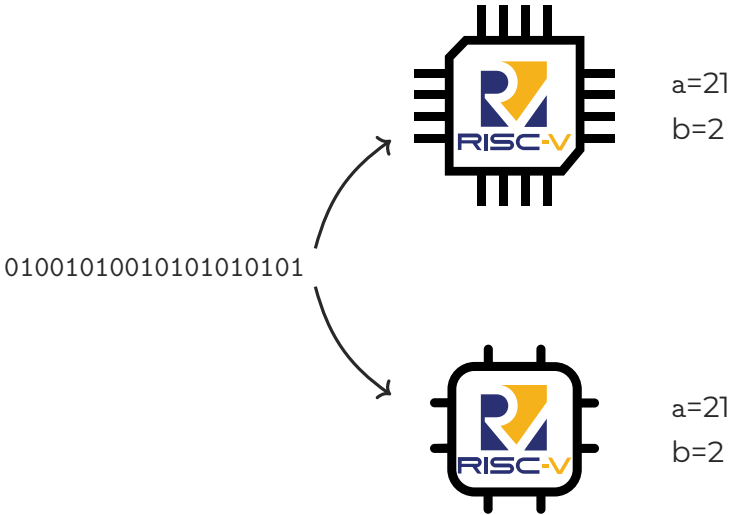

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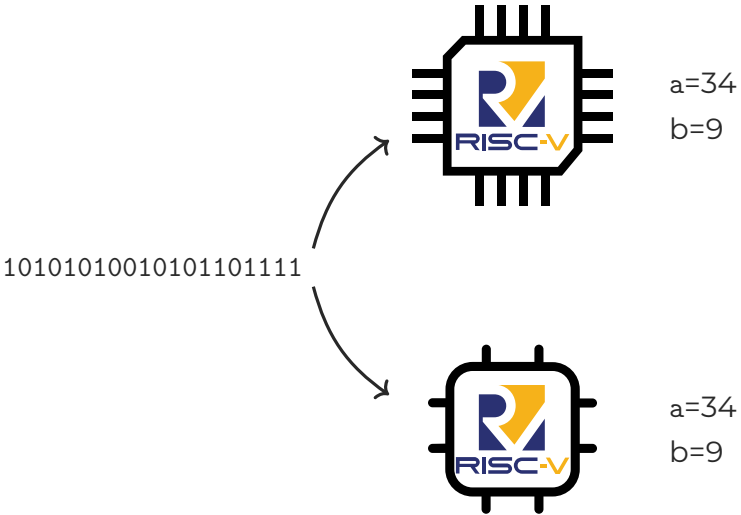

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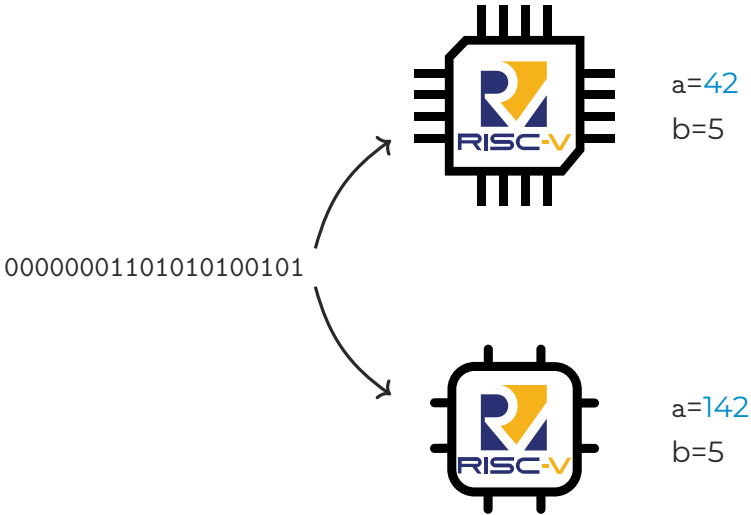

Intel F00F Bug

A single (invalid) instruction deadlocked the CPU

Halt and Catch Fire (C906)

```
th.lbib t0, (t0), 0, 0
frcsr t0
li t0, 0
```

Halt and Catch Fire (C906)

```
th.lbib t0, (t0), 0, 0
frcsr t0
li t0, 0
```

CPU just hangs

Halt and Catch Fire (C906)

```
th.lbib t0, (t0), 0, 0
frcsr t0
li t0, 0
```

Synopsis

Load indexed byte, increment address before loading.

Mnemonic

`th.lbib rd, (rs1), imm5, imm2`

Description

This instruction increments the value in `rs1` by (`sign_extend(imm5)` « `imm2`) and writes the result back to `rs1`. After the increment of `rs1`, this instruction loads a sign extended 8-bit value into the GP register `rd` from the (incremented) address `rs1`.

The encoding of this instruction with equal rd and rs1 is reserved.

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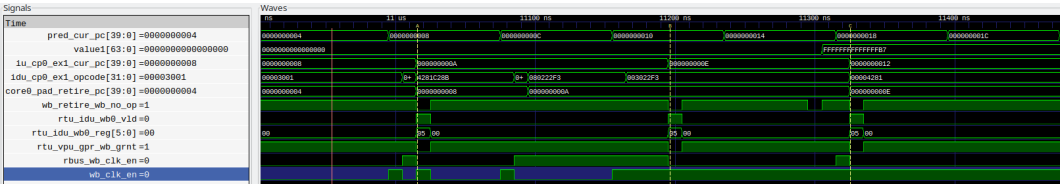

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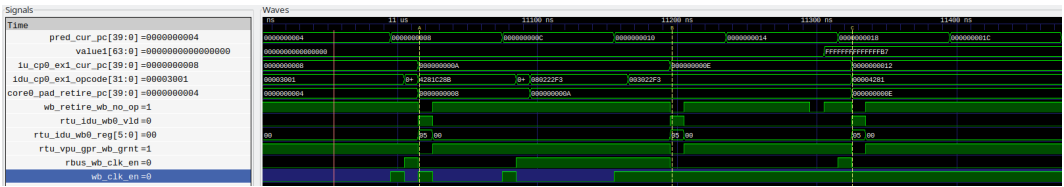


```
**********************************************************************
* Error: There is no instructions retired in the last 50000 cycles! *
*                Simulation Fail and Finished!                       *
**********************************************************************
```

Other Cores?

```
.fill 1, 4, 0x20b00087
```

T-Head C908

Other Cores?

```
.fill 1, 4, 0x20b00087
```

T-Head C908

```
.fill 1, 4, 0xe0815407
```

SpacemiT X60

Mitigation Options

C908/X60 DoS

- Disable V extension in kernel
- Prevents denial-of-service on C908/X60

👎 Performance loss

👎 Breaks vector-dependent software

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C906 DoS

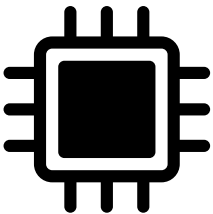
- T-Head vendor extension cannot be disabled
- “The th.sxstatus.THEADISAEE bit is not expected to be cleared. The behavior of clearing this bit is undefined”.

⚠ No known mitigation

GhostWrite

RISC-V Vector Instructions

```
vse128.v v0, 0(t0)
```



t0	v0	v1	v2
0x1000	RISC-V␣is␣a␣super	r␣cool␣CPU␣archi	tecture!

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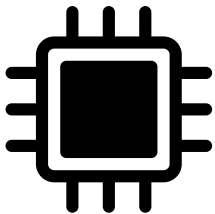

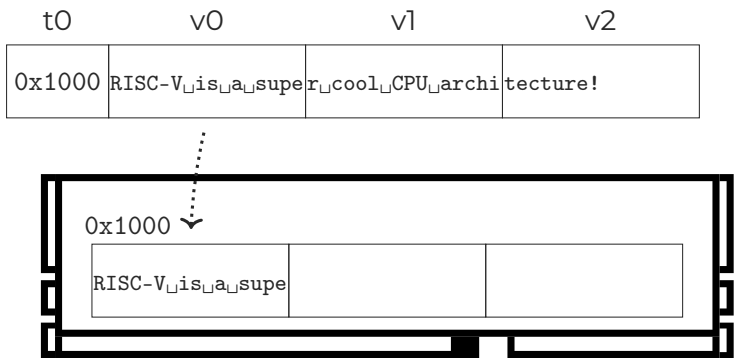

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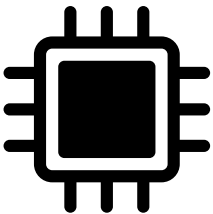

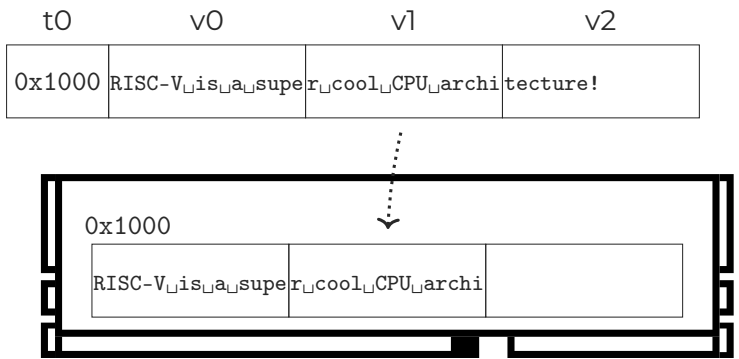

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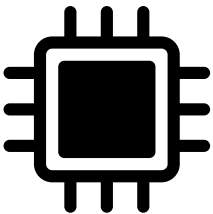
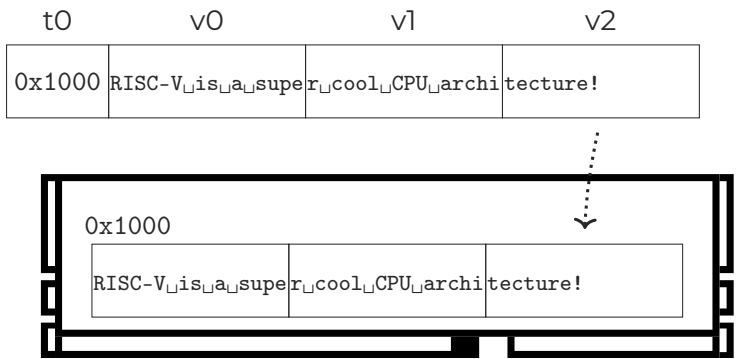
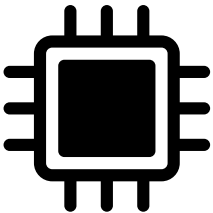
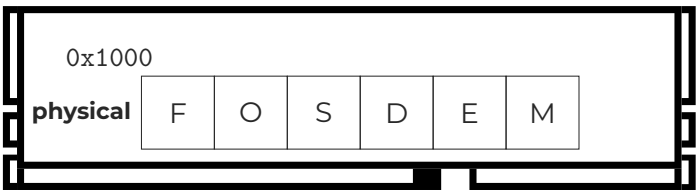




RISC-V Flawed Vector Instruction (C910)



t0	v0	v1	v2	v3	v4	v5
0x1000	R	I	S	C	-	V



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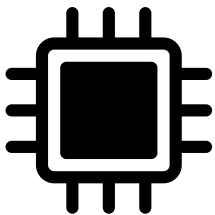

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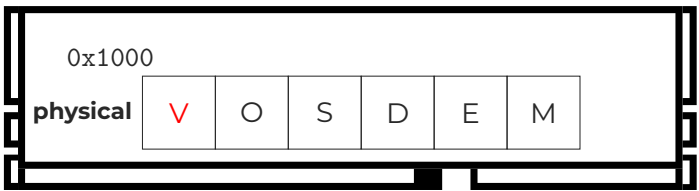

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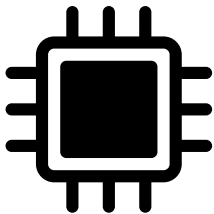

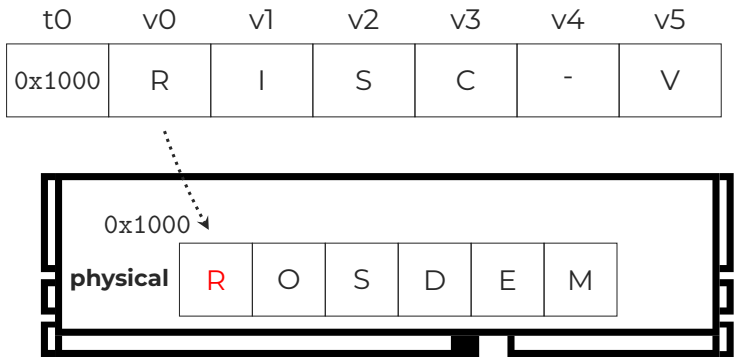

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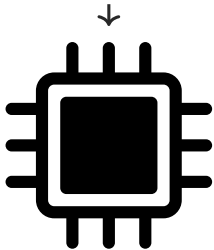

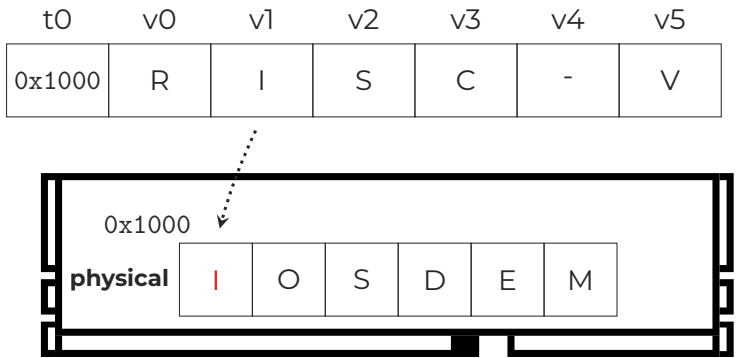

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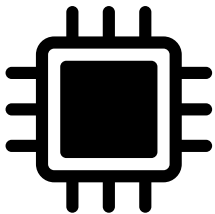

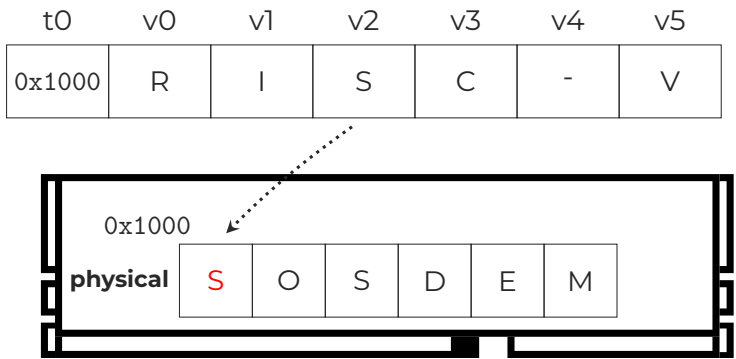

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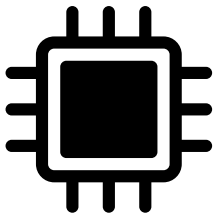

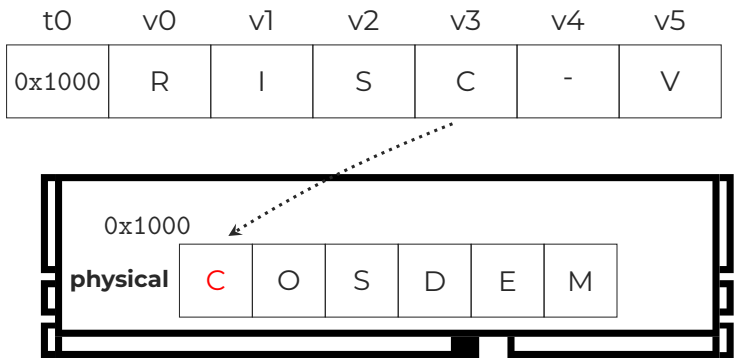

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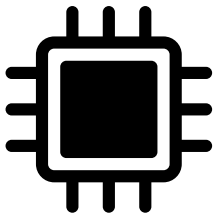

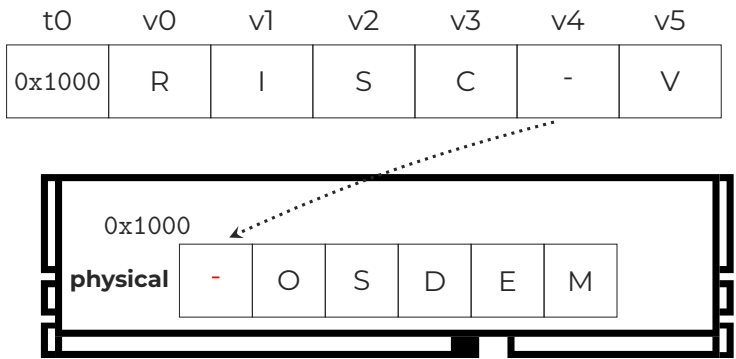

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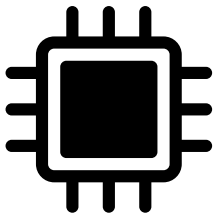
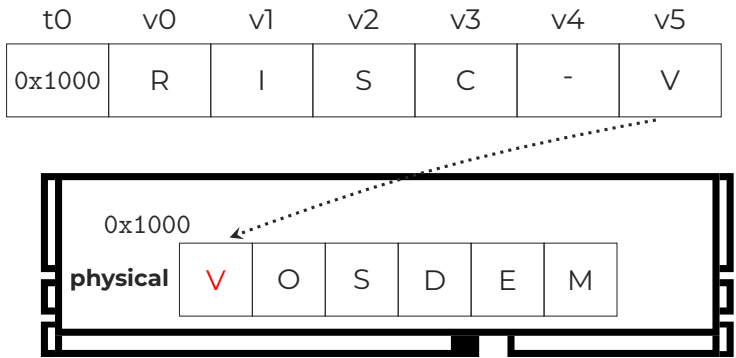
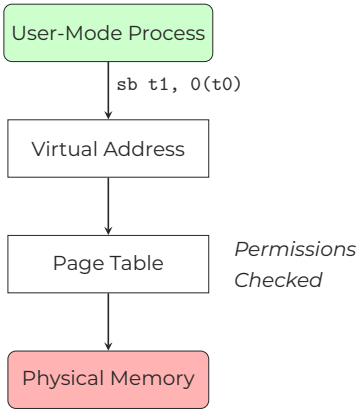




GhostWrite: Circumventing Virtual Memory

Normal Memory Write



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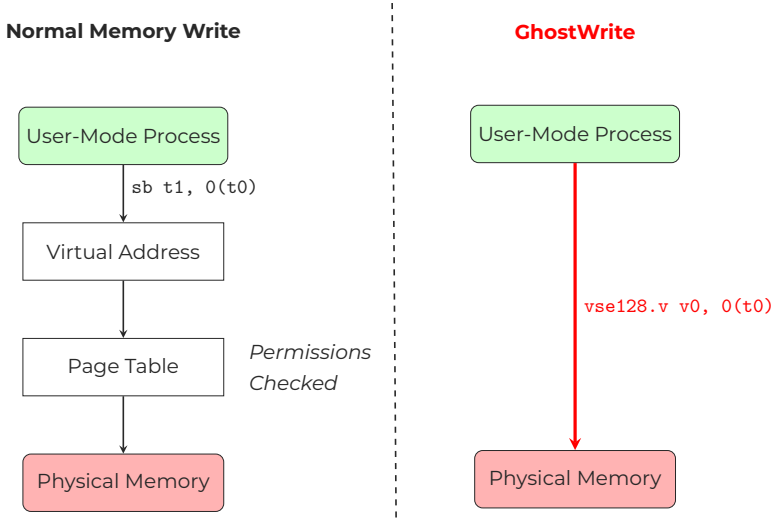

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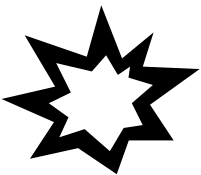
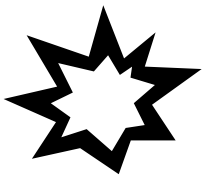


Rewrite page tables

Overwrite kernel

GhostWrite Exploitation



Rewrite page tables

Overwrite kernel

Modify M-mode firmware

Break trusted execution


unprivileged@c910:~$

Elastic Metal RV1

The world's first RISC-V servers available in the cloud.
Taste the new open processor architecture now.
Will you take the risk?

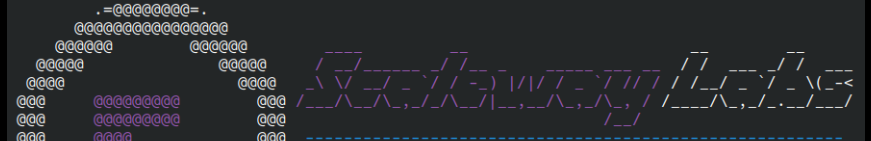
Order Now →

Read the press release →

An open RISC architecture

Compact and economical

Designed and assembled in Paris




```
Welcome to Ubuntu 23.10 (GNU/Linux 5.10.113+ riscv64)

 * Documentation:  https://help.ubuntu.com
 * Management:     https://landscape.canonical.com
 * Support:        https://ubuntu.com/advantage


0 updates can be applied immediately.


Last login: Sat Mar  9 14:16:33 2024 from 87.145.163.240
ubuntu@risc:~$ sudo ./a.out
Virtual address:        3feab9f000
Phyiscal address:        3efc9b000

Value before:                caaa
Value after:                 cafe
ubuntu@risc:~$
```

GhostWrite Mitigation Options

Disable Vector Extension

- Disable V extension in kernel
- Blocks GhostWrite

👎 Performance loss

👎 No software relying on V

👎 Requires trusted kernel

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```
Vulnerabilities:
  Gather data sampling:      Not affected
  Ghostwrite:                Mitigation; xtheadvector disabled
  Indirect target selection: Not affected
  Itlb multihit:             Not affected
  L1tf:                      Not affected
  Mds:                       Not affected
  Meltdown:                  Not affected
  Mmio stale data:           Not affected
  Reg file data sampling:    Not affected
  Retbleed:                  Not affected
```

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Replace CPU

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Trade off: short-term software band aid (disable V) versus long-term architectural fix (new CPU revision).

Patterns From our Findings

Limited DV Scrutiny

- Hardware $\neq$ Software $\rightarrow$ DV is critical
- Differential testing across vendors

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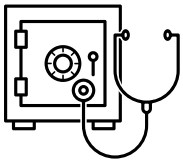
- Implement only ratified extensions
- Use vendor extensions carefully
- Mandate specific behavior in ISA

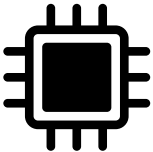
No Update Path

- Microcode or similar mechanism
- Even if microcode adds complexity
- We argue: Increases security

CPU Vulnerability Classes



Side Channels



CPU Bugs

Transient Execution

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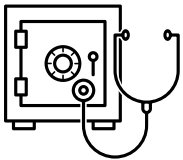

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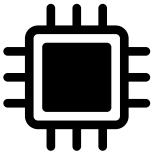

CPU Bugs

Transient Execution

```
lgerlach@lab53 ..eculate/experiments/pocs/e2e/userspace % CENSOR_HASHES=1 sudo -E ./hash_lookup_bpf /etc/shadow
```

Spectre on RISC-V: Implications

Out-of-order RISC-V CPUs are vulnerable to Spectre

Kernel lacks mitigations that x86 and ARM have had since 2018

No Speculation Barriers

x86

`LFENCE`

Standardized

ARM

`CSDB` / `DSB`

Standardized

RISC-V

Nothing

No dedicated fence

No Speculation Barriers

x86

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Standardized

RISC-V

Nothing

No dedicated fence

- BPF JIT has no instruction to emit → emits no-op
- Workaround: CSR reads (`rdtime`) empirically stop speculation
- But: undocumented behavior, not guaranteed

Kernel Patches

Unprotected kernel paths on RISC-V

- Syscall dispatch – no `array_index_nospec`
- User memory access – no pointer masking
- BPF – JIT does not emmit speculation barrier
- Futex operations

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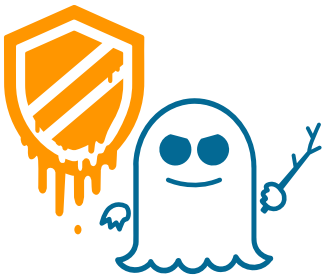
Patches submitted – some already merged into Linux mainline

What we need to mitigate this



- Standardized serializing fence instruction needed
- Kernel needs fine grained settings for mitigations
- Compiler needs support for retpoline equivalent
- Vendors need to document speculative behavior of CPUs

What goes wrong

- Unprivileged timers & cache maintenance
- Vendor extensions, non-ratified extensions
- Bugs: GhostWrite, DoS
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`github.com/cispa/Security-RISC`

`github.com/cispa/RISCover`

Security Problem or Not?

CVE-2025-20103 (DoS)

Insufficient resource pool in the core management mechanism for some Intel Processors may allow an authenticated user to potentially enable denial of service via local access.

6.5 Medium

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6.5 Medium

CVE-2017-5754 (Meltdown)

Systems with microprocessors utilizing speculative execution and indirect branch prediction may allow unauthorized disclosure of information to an attacker with local user access via a side-channel analysis of the data cache.

5.6 Medium

Simple, but Effective

Small tests. Big failures.

Real bugs found in seconds or minutes across diverse RISC-V cores.

Privilege Escalation

C910, C920

<1 second

Denial-of-Service

C906, C908, X60

2–50 minutes

Architectural Bugs

U54, P550, C906, C908, C910

<2 minutes

Simulator Breakage

QEMU segfaults

<30 seconds