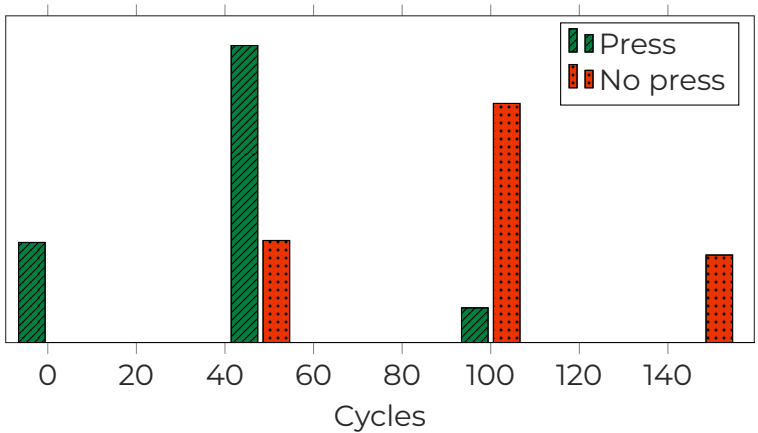
CISPA
HELMHOLTZ CENTER FOR INFORMATION SECURITY

# RISCy Cache Coherence

*Timer-Free Architectural Cache Attacks via Instruction/Data Cache Incoherence*

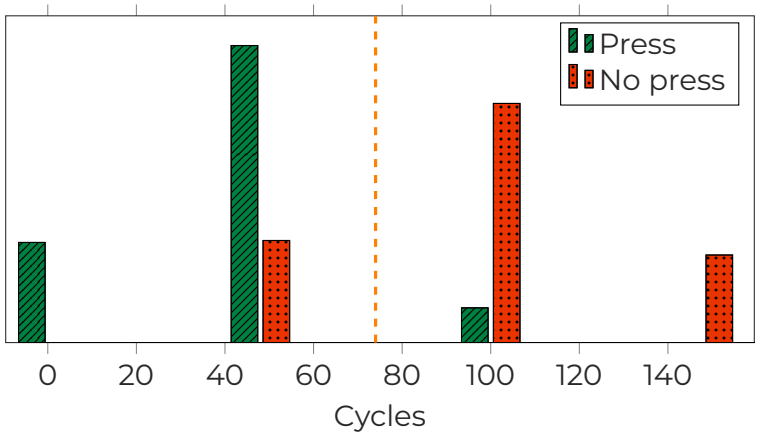
**Fabian Thomas**, Michael Schwarz

# Where do you draw the line?



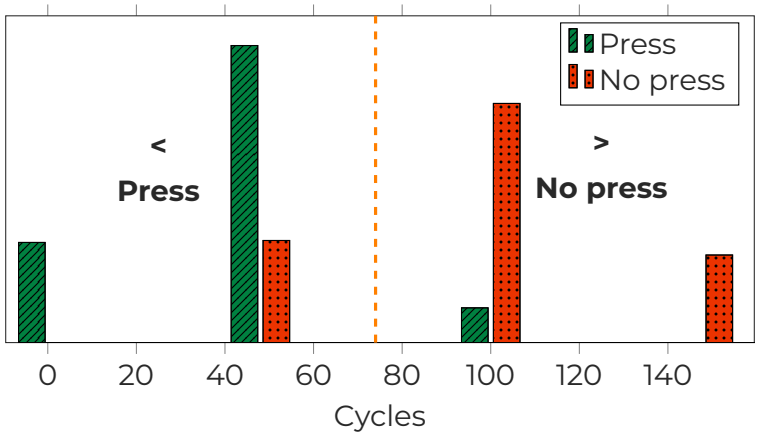

Qualcomm Snapdragon X (Oryon)

# Where do you draw the line?



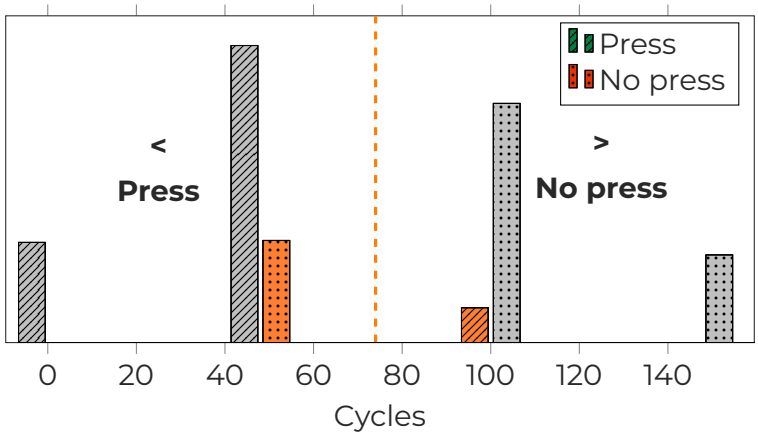

Qualcomm Snapdragon X (Oryon)

# Where do you draw the line?




Qualcomm Snapdragon X (Oryon)

# Where do you draw the line?



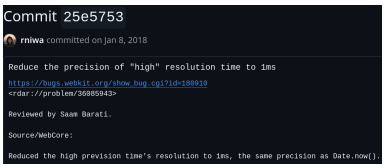

Qualcomm Snapdragon X (Oryon)

To offer protection against timing attacks and fingerprinting, `performance.now()` is coarsened based on whether or not the document is cross-origin isolated.

- Resolution in isolated contexts: 5 microseconds
- Resolution in non-isolated contexts: 100 microseconds

Before version 91, timer resolutions in Chrome were restricted to 5 microseconds on desktop, where site-isolation is enabled, and to 100 microseconds on Android, where it's not.

Starting from version 91, following a specification change, Chrome will be restricting the resolution of explicit timers (`performance.now()`, `performance.timeOrigin`, and other performance APIs that expose `DOMHighResTimestamps`) to 100 microseconds across platforms. By enabling cross-origin isolation, websites can relax the restriction to 5 microseconds regardless of platform.

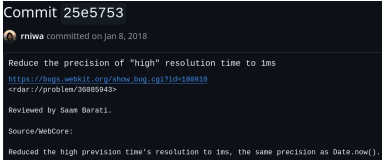


To offer protection against timing attacks and fingerprinting, `performance.now()` is coarsened based on whether or not the document is cross-origin isolated.

- Resolution in isolated contexts: 5 microseconds
- Resolution in non-isolated contexts: 100 microseconds

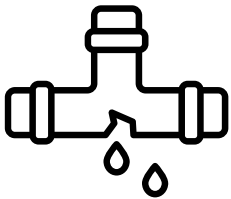
Before version 91, timer resolutions in Chrome were restricted to 5 microseconds on desktop, where site-isolation is enabled, and to 100 microseconds on Android, where it's not.

Starting from version 91, following a specification change, Chrome will be restricting the resolution of explicit timers (`performance.now()`, `performance.timeOrigin`, and other performance APIs that expose `DOMHighResTimestamps`) to 100 microseconds across platforms. By enabling cross-origin isolation, websites can relax the restriction to 5 microseconds regardless of platform.




## Solution: Timer-Free Side Channels

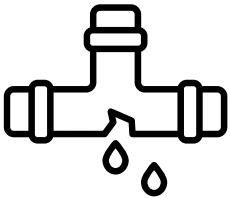
# I²SC: Instruction-Cache Incoherence Side Channel



**Building Block 1**

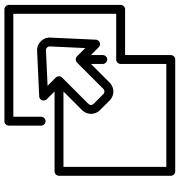
Leak I-cache state via I/D-Cache Incoherence

# I²SC: Instruction-Cache Incoherence Side Channel



**Building Block 1**

Leak I-cache state via I/D-Cache Incoherence

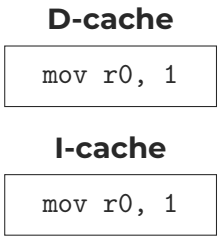


**Building Block 2**

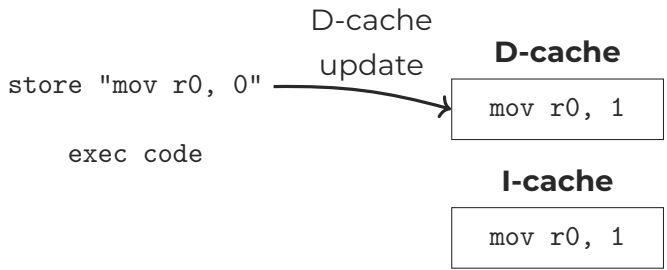
Transfer cache state of D-cache line to I-cache line

# B1: Leaking I-Cache State Without Timers

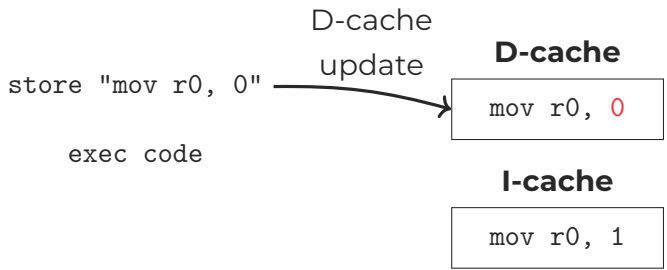
```
store "mov r0, 0"

    exec code
```



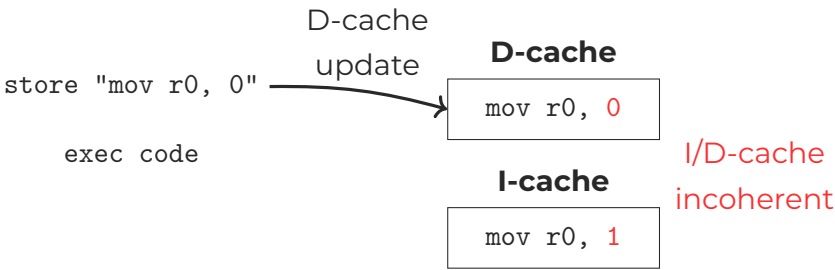
# B1: Leaking I-Cache State Without Timers



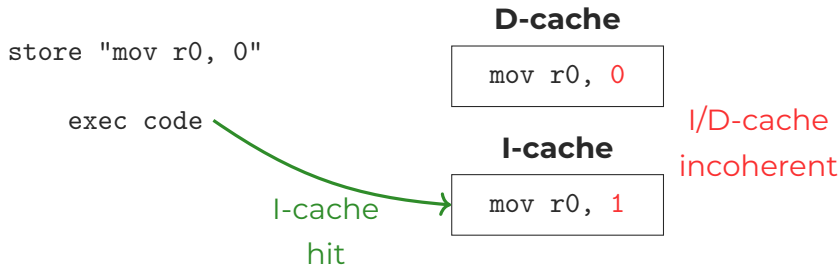
# B1: Leaking I-Cache State Without Timers



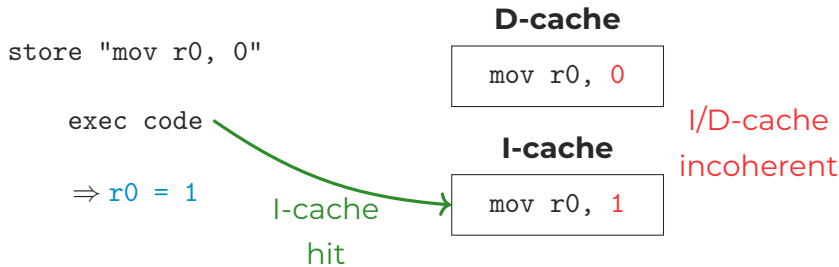
# B1: Leaking I-Cache State Without Timers



# B1: Leaking I-Cache State Without Timers

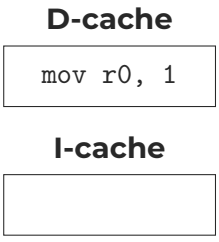


# B1: Leaking I-Cache State Without Timers

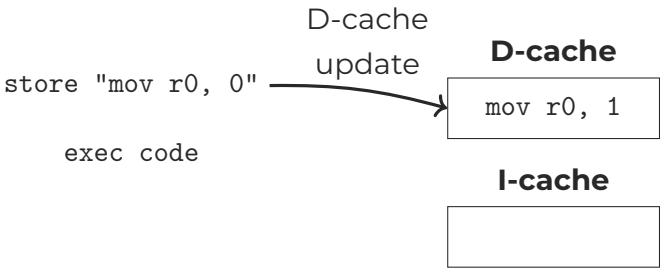


# B1: Leaking I-Cache State Without Timers

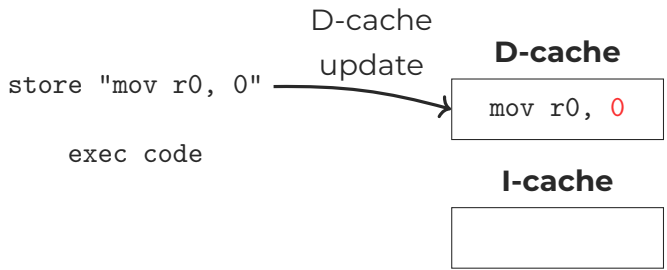
```
store "mov r0, 0"

    exec code
```



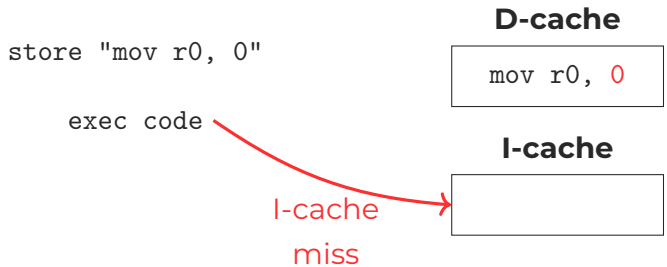
# B1: Leaking I-Cache State Without Timers



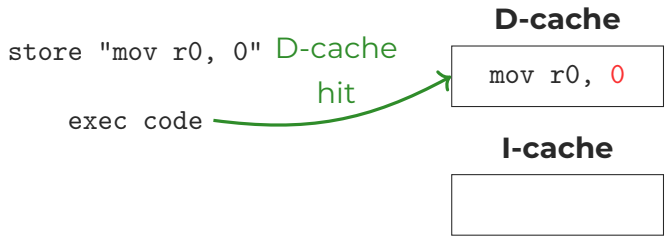
# B1: Leaking I-Cache State Without Timers



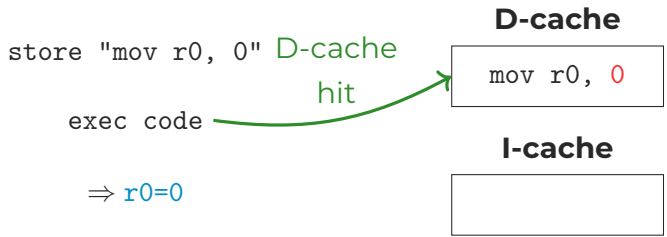
# B1: Leaking I-Cache State Without Timers



# B1: Leaking I-Cache State Without Timers



# B1: Leaking I-Cache State Without Timers



# B1: Leaking I-Cache State Without Timers

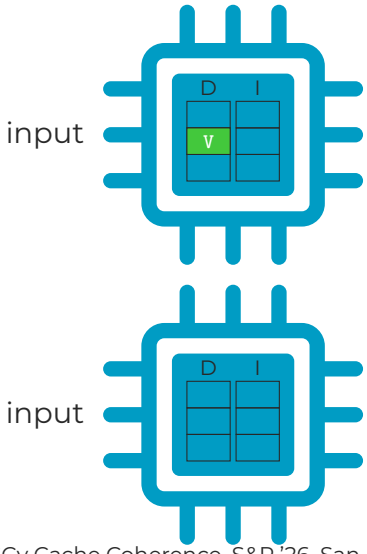

**code in I-cache** ⇔ `r0 = 1`

# B1: Leaking I-Cache State Without Timers

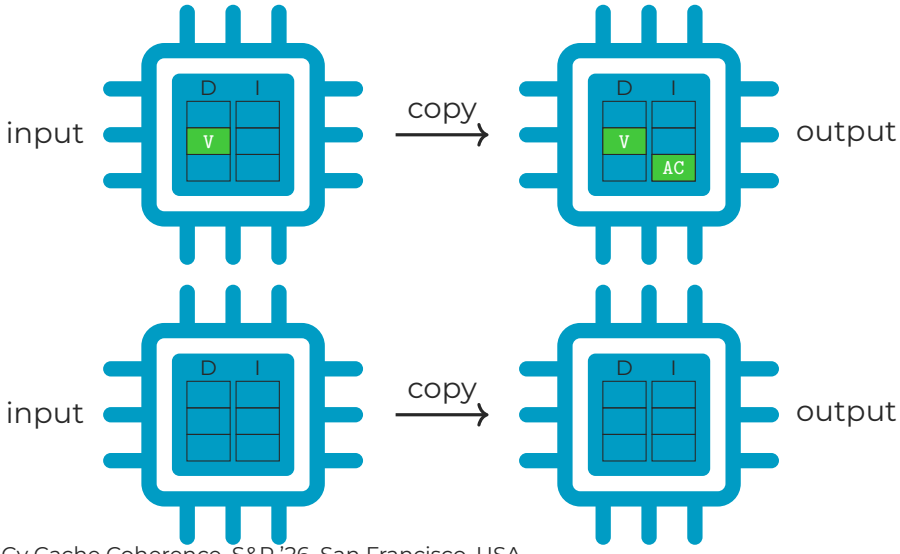
| Architecture | ARM | | | | | | | | | | | | | | RISC-V | | | | LoongArch |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Vendor | ARM | | | | | | | | | Qualcomm | | Huawei | Apple | | T-Head | | | SpacemiT | Loongson |
| Microarchitecture | Cortex-A520 | Cortex-A72 | Cortex-A73 | Cortex-A76 | Cortex-A78 | Cortex-A720 | Cortex-A725 | Cortex-X4 | Neoverse-N1 | Oryon | | Kunpeng Pro | Icestorm | Firestorm | C906 | C908 | C910 | X60 | 3A5000-HV |
| Building Blocks | ◐ | ○ | ◐ | ◐ | ◐ | ◐ | ◐ | ◐ | ◐ | ◐ | | ◐ | ◐ | ◐ | ○ | ◐ | ◐ | ◐ | ◐ |

◐ = B1 works.

# B2: Cache-State Transfer Gadget



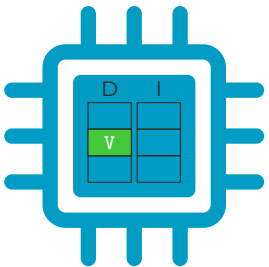
# B2: Cache-State Transfer Gadget



# B2: Cache-State Transfer Gadget

```
LOAD LR, [X2]
RETURN
LOAD X2, VICTIM
BRANCH ATTACKER_CODE+X2
```

Misprediction triggers transient execution

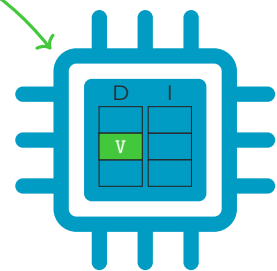


# B2: Cache-State Transfer Gadget

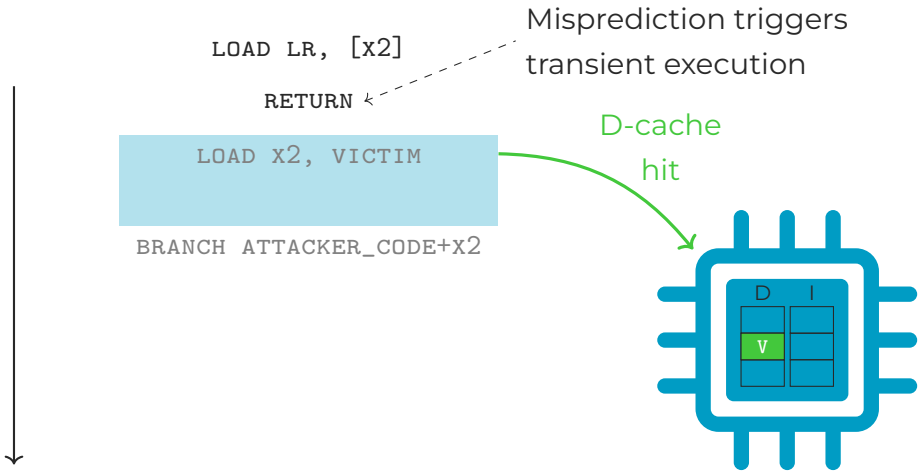
```
LOAD LR, [X2]
RETURN
LOAD X2, VICTIM
BRANCH ATTACKER_CODE+X2
```

Misprediction triggers transient execution

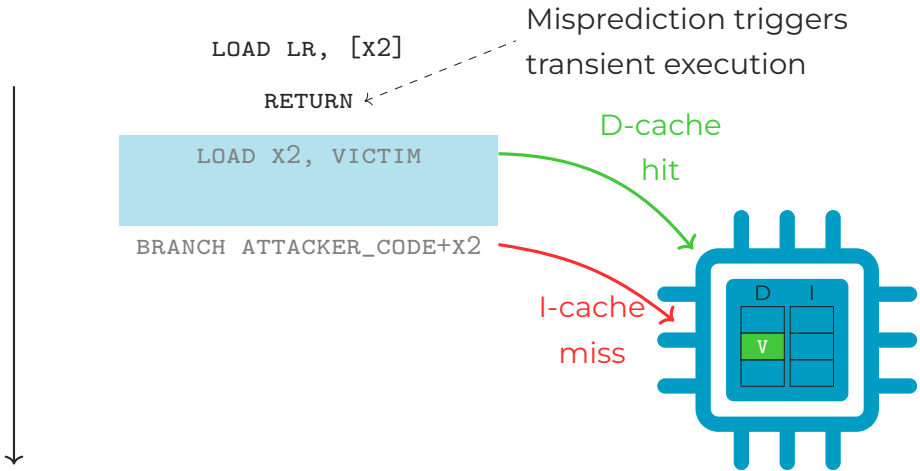
D-cache hit



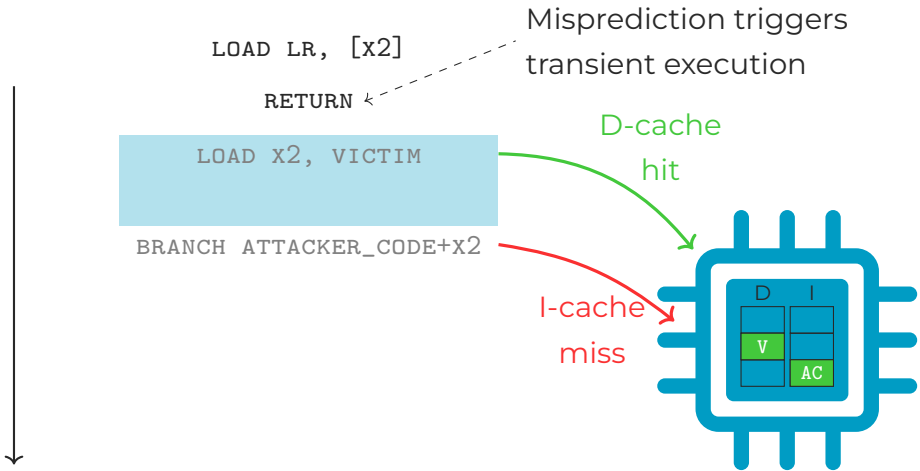
# B2: Cache-State Transfer Gadget



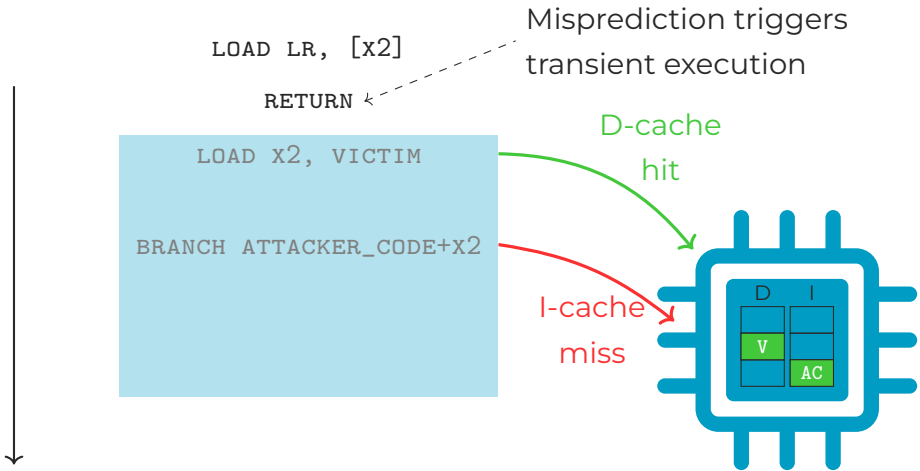
# B2: Cache-State Transfer Gadget



# B2: Cache-State Transfer Gadget



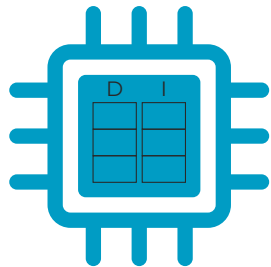
# B2: Cache-State Transfer Gadget



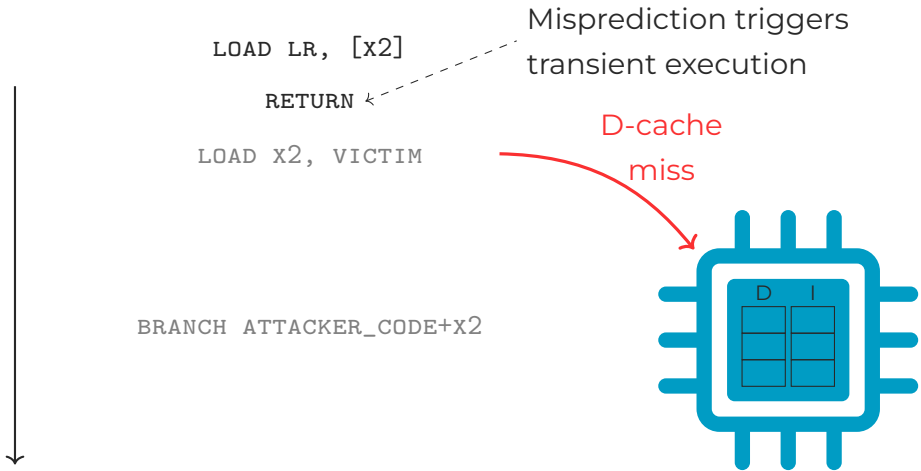
# B2: Cache-State Transfer Gadget

```
LOAD LR, [X2]
RETURN
LOAD X2, VICTIM
BRANCH ATTACKER_CODE+X2
```

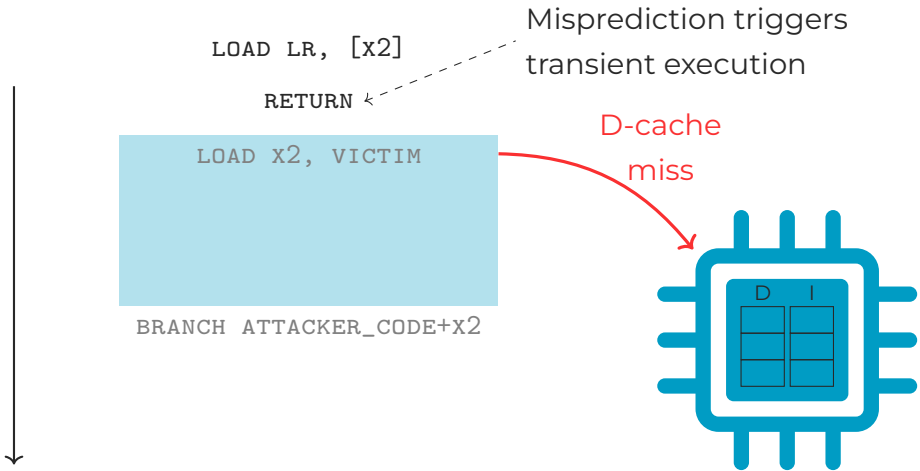
Misprediction triggers transient execution



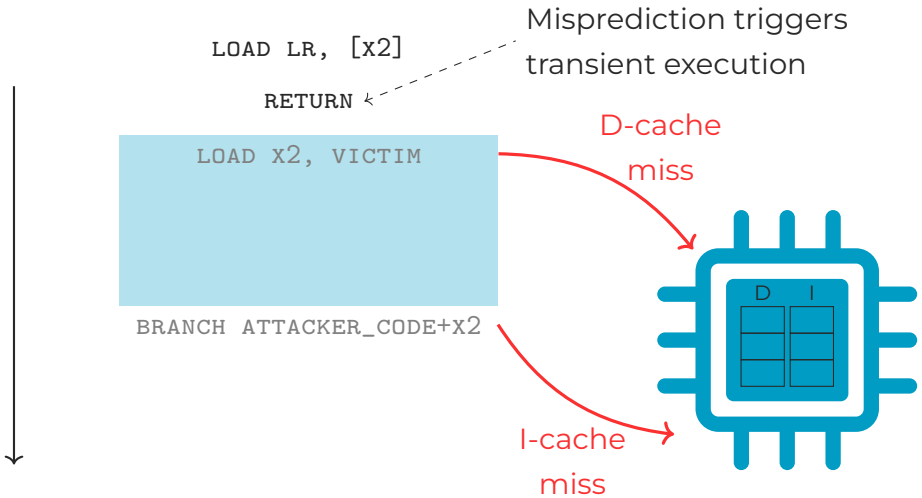
# B2: Cache-State Transfer Gadget



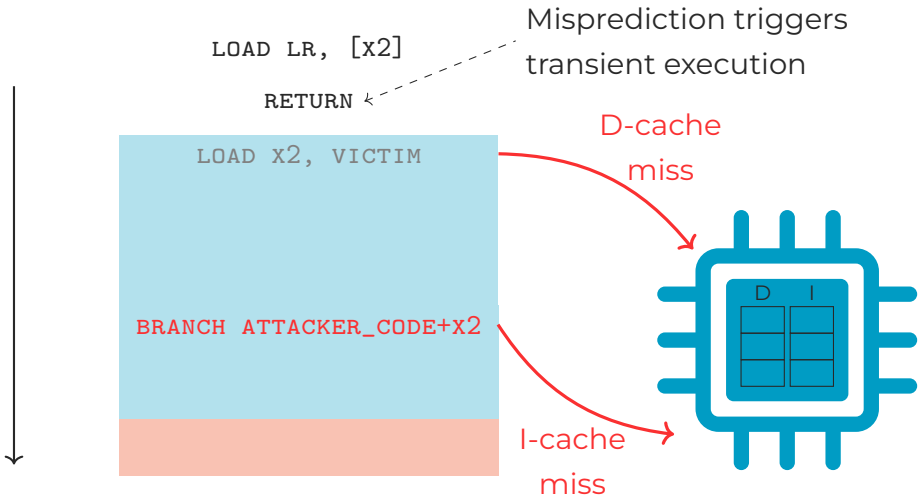
# B2: Cache-State Transfer Gadget



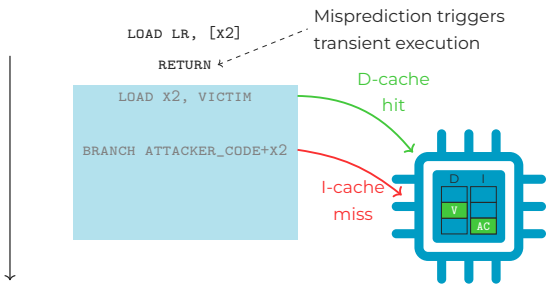
# B2: Cache-State Transfer Gadget

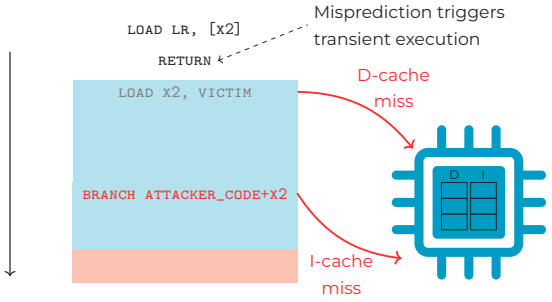


# B2: Cache-State Transfer Gadget



# B2: Cache-State Transfer Gadget




**victim in cache ⟺ attacker code in cache**

# B2: Cache-State Transfer Gadget

| Architecture | ARM | | | | | | | | | | | | | RISC-V | | | | LoongArch |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Vendor | ARM | | | | | | | | | Qualcomm | | Huawei | Apple | T-Head | | | SpacemiT | Loongson |
| Microarchitecture | Cortex-A520 | Cortex-A72 | Cortex-A73 | Cortex-A76 | Cortex-A78 | Cortex-A720 | Cortex-A725 | Cortex-X4 | Neoverse-N1 | Oryon | | Kunpeng Pro | Icestorm | Firestorm | C906 | C908 | C910 | X60 | 3A5000-HV |
| Building Blocks | ○ | ◑ | ○ | ◑ | ◑ | ◑ | ◑ | ◑ | ◑ | ◑ | | ◑ | ◑ | ◑ | ○ | ○ | ◑ | ○ | ◑ |

◑ = B2 works.

# I²SC: Instruction-Cache Incoherence Side Channel

| Architecture | ARM | | | | | | | | | | | | | RISC-V | | | | LoongArch |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Vendor | ARM | | | | | | | | Qualcomm | | Huawei | Apple | | T-Head | | | SpacemiT | Loongson |
| Microarchitecture | Cortex-A520 | Cortex-A72 | Cortex-A73 | Cortex-A76 | Cortex-A78 | Cortex-A720 | Cortex-A725 | Cortex-X4 | Neoverse-N1 | Oryon | | Kunpeng Pro | Icestorm | Firestorm | C906 | C908 | C910 | X60 | 3A5000-HV |
| Building Blocks | ◐ | ◑ | ◐ | ● | ● | ● | ● | ● | ● | ● | | ● | ● | ● | ○ | ◐ | ● | ◐ | ● |
| I²SC | | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | ✓ | | | ✓ | | ✓ |

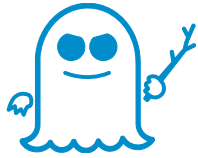
◐ = B1 works; ◑ = B2 works; ● / ✓ = I²SC works.

# Case Studies

AES T-table
key recovery,
**100%** (Ours) vs.
**1%** (Flush+Reload)

# Case Studies

AES T-table
key recovery,
**100%** (Ours) vs.
**1%** (Flush+Reload)



Spectral attacks,
first on: RISC-V and
LoongArch

# Case Studies

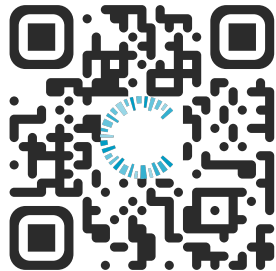
AES T-table
key recovery,
**100%** (Ours) vs.
**1%** (Flush+Reload)

Spectral attacks,
first on: RISC-V and
LoongArch

Side-Channel Attack
on Android shared
library (Pixel 9)

# Summary

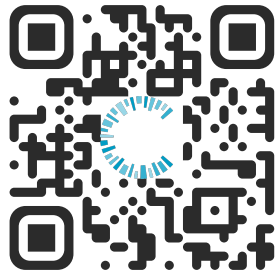
- Modern systems **restrict timers**



s.roots.ec/riscy

# Summary

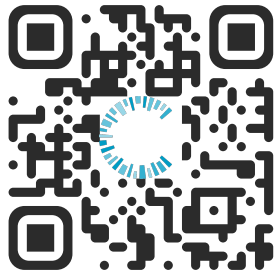
- Modern systems **restrict timers**
- I$^2$SC is a **timer-free alternative** for classical side-channel attacks on the D-cache



s.roots.ec/riscy

# Summary

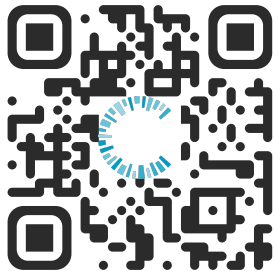
- Modern systems **restrict timers**
- I$^2$SC is a **timer-free alternative** for classical side-channel attacks on the D-cache
- Building Block 1: Use **D/I-cache incoherence** as side channel



s.roots.ec/riscy

# Summary

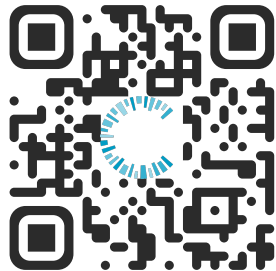
- Modern systems **restrict timers**
- I²SC is a **timer-free alternative** for classical side-channel attacks on the D-cache
- Building Block 1: Use **D/I-cache incoherence** as side channel
- Building Block 2: **Transfer cache state** of D-cache line to I-cache line



s.roots.ec/riscy

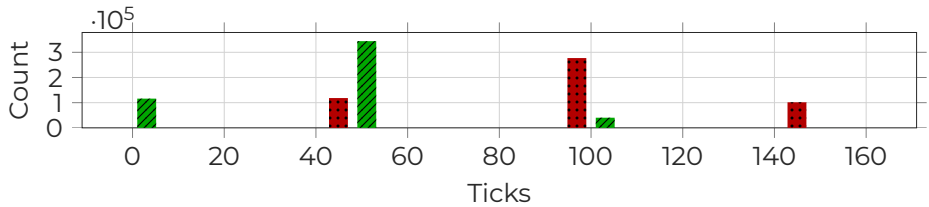
# Summary

- Modern systems **restrict timers**
- I$^2$SC is a **timer-free alternative** for classical side-channel attacks on the D-cache
- Building Block 1: Use **D/I-cache incoherence** as side channel
- Building Block 2: **Transfer cache state** of D-cache line to I-cache line
- Available on **12 microarchitectures** across **3 RISC ISAs** (ARM, RISC-V, LoongArch)

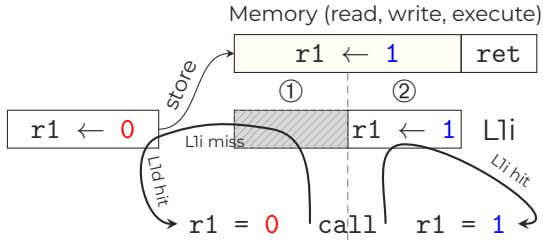


s.roots.ec/riscy

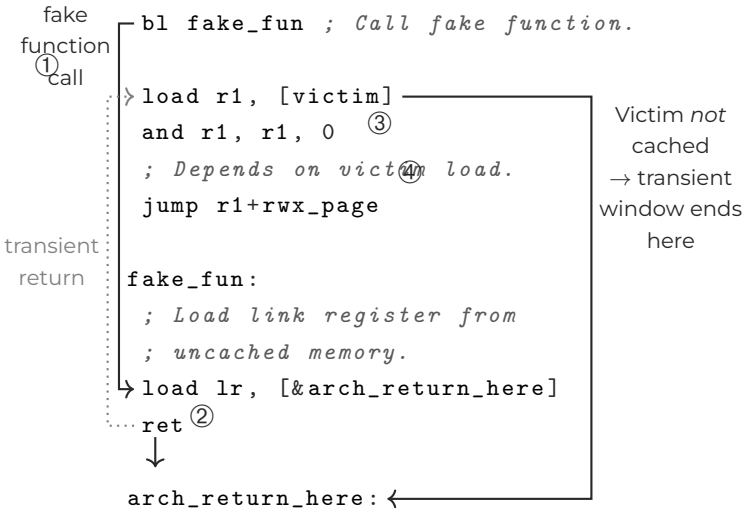
# Timer Histogram (Oryon)



# I²SC Overview



# Cache-State Copier Gadget



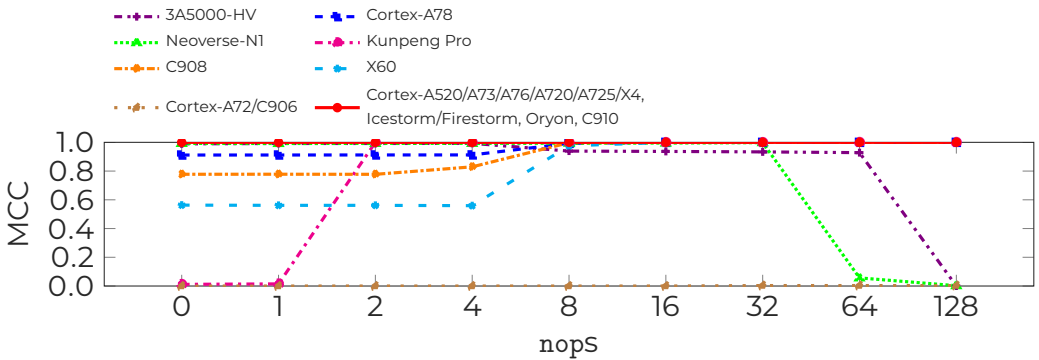
# Devices

| ISA | Microarchitecture | Device | SoC | RAM | OS |
|---|---|---|---|---|---|
| ARM | Cortex-A520 | Google Pixel 9 | Google Tensor G4 | 12GB | Android 16 |
| | Cortex-A72 | MOCHAbin 5G | Marvell ARMADA | 8GB | Ubuntu 18.04.6 LTS |
| | Cortex-A73 | ODROID-N2+ | Amlogic S922X | 4GB | Ubuntu 20.04.5 LTS |
| | Cortex-A76 | NanoPi R6S | Rockchip RK3588S | 8GB | Ubuntu 22.04.2 LTS |
| | Cortex-A78 | Radxa NIO 12L | MediaTek Genio 1200 | 16GB | Rity Demo Layer 23.2-release (kirkstone) |
| | Cortex-A720 | Google Pixel 9 | Google Tensor G4 | 12GB | Android 16 |
| | Cortex-A725 | Poco X7 Pro | Mediatek Dimensity 8400 Ultra | 8GB | Android 15 |
| | Cortex-X4 | Google Pixel 9 | Google Tensor G4 | 12GB | Android 16 |
| | Neoverse-N1 | Ampere Altra Q64-30 | Ampere Altra Q64-30 | 64GB | Ubuntu 24.04.2 LTS |
| | Oryon | Lenovo ThinkCentre Neo 50q QC | Snapdragon X (X1-26-100) | 16GB | Microsoft Windows 11 Pro |
| | Kunpeng Pro | OrangePi Kunpeng Pro | Huawei Kunpeng | 16GB | openEuler 22.03 (LTS-SP3) |
| | Icestorm | Apple MacBook (M1) | Apple M1 | 16GB | Arch Linux ARM |
| | Firestorm | Apple MacBook (M1) | Apple M1 | 16GB | Arch Linux ARM |
| RISC-V | C906 | Lichee RV Dock | Allwinner D1 | 1GB | Ubuntu 24.04 LTS |
| | C908 | youyeetoo CanMV-K230 | Kendryte K230 | 1GB | Debian GNU/Linux trixie/sid |
| | C910 | LicheePi 4A | T-Head TH1520 | 8GB | Debian GNU/Linux 12 (bookworm) |
| | X60 | Banana Pi BPI-F3 | SpacemiT K1 | 4GB | Armbian-bpi-SpacemiT 24.5.0-trunk sid |
| LoongArch | 3A5000-HV | Loongson 3A5000 | Loongson 3A5000 | 32GB | Loongnix GNU/Linux 20 (DaoXiangHu) |

# Forwarding Test

```
; initially [rwx_page] = mov reg1, 1; ret
store mov_reg1_0, [rwx_page]
memory barrier ; optional
N * nop ; N=1<<k, 0<=k<=15
jump rwx_page
; observe architectural result in reg1
store mov_reg1_0, [overwrite_here]
memory barrier ; optional
N * nop ; N=1<<k, 0<=k<=15
overwrite_here:
mov reg1, 1
; observe architectural result in reg1
```

# Propagation Test



# Transient Fetch Evaluation

| Microarch. | Data Load uncached | Data Load cached | Instr. Fetch uncached | Instr. Fetch cached | B2 |
|---|---|---|---|---|---|
| Cortex-A72 |  |  |  |  | ✓ |
| Cortex-A73 |  |  |  |  | |
| Cortex-A76 |  |  |  |  | ✓ |
| Cortex-A78 |  |  |  |  | ✓ |
| Cortex-A720 |  |  |  |  | ✓ |
| Cortex-A725 |  |  |  |  | ✓ |
| Cortex-X4 |  |  |  |  | ✓ |
| Neoverse-N1 |  |  |  |  | ✓ |
| Oryon |  |  |  |  | ✓ |
| Kunpeng Pro |  |  |  |  | ✓ |
| Icestorm |  |  |  |  | ✓ |
| Firestorm |  |  |  |  | ✓ |
| C910 |  |  |  |  | ✓ |
| 3A5000-HV |  |  |  |  | ✓ |

# B1 Covert Channel

| | Error Rate (%, ↓) | | | Throughput (kbit s$^{-1}$, ↑) | | | Resolution (µs, ↓) | | |
|---|---|---|---|---|---|---|---|---|---|
| **Microarch.** | **Timer** | **B1** | **Δ** | **Timer** | **B1** | **Δ%** | **Timer** | **B1** | **Δ%** |
| Cortex-A520 | 2.83 | 0.00 | -2.8 | 615.21 | 777.95 | +26.5 | 1.63 | 1.29 | -20.9 |
| Cortex-A73 | 0.01 | 0.18 | +0.2 | 956.99 | 1410.35 | +47.4 | 1.04 | 0.71 | -31.7 |
| Cortex-A76 | 15.79 | 0.03 | -15.8 | 889.83 | 1036.97 | +16.5 | 1.12 | 0.96 | -14.3 |
| Cortex-A78 | 1.32 | 0.00 | -1.3 | 1360.69 | 1712.61 | +25.9 | 0.73 | 0.58 | -20.5 |
| Cortex-A720 | 2.67 | 0.00 | -2.7 | 922.13 | 1212.07 | +31.4 | 1.08 | 0.83 | -23.1 |
| Cortex-A725 | 0.67 | 0.00 | -0.7 | 481.46 | 539.06 | +12.0 | 2.08 | 1.86 | -10.6 |
| Cortex-X4 | 12.89 | 0.04 | -12.9 | 1343.73 | 1547.63 | +15.2 | 0.74 | 0.65 | -12.2 |
| Neoverse-N1 | 1.66 | 0.15 | -1.5 | 756.59 | 842.06 | +11.3 | 1.32 | 1.19 | -9.8 |
| Oryon | 17.76 | 0.00 | -17.8 | 925.73 | 1905.49 | +105.8 | 1.08 | 0.52 | -51.9 |
| Kunpeng Pro | 0.01 | 0.03 | +0.0 | 618.42 | 684.64 | +10.7 | 1.62 | 1.46 | -9.9 |
| Icestorm | 0.02 | 0.00 | -0.0 | 1100.62 | 1277.07 | +16.0 | 0.91 | 0.78 | -14.3 |
| Firestorm | 0.05 | 0.00 | -0.1 | 1372.07 | 1534.83 | +11.9 | 0.73 | 0.65 | -11.0 |
| C908 | 0.61 | 0.20 | -0.4 | 913.77 | 824.89 | -9.7 | 1.09 | 1.21 | +11.0 |
| C910 | 30.69 | 0.07 | -30.6 | 542.79 | 538.74 | -0.7 | 1.84 | 1.86 | +1.1 |
| X60 | 1.13 | 1.26 | +0.1 | 213.68 | 211.55 | -1.0 | 4.68 | 4.73 | +1.1 |
| 3A5000-HV | 0.01 | 0.36 | +0.3 | 2846.13 | 2961.38 | +4.0 | 0.35 | 0.34 | -2.9 |

# B2 Covert Channel

| | Error Rate (%, ↓) | | | Throughput (kbit s$^{-1}$, ↑) | | | Resolution (µs, ↓) | | |
|---|---|---|---|---|---|---|---|---|---|
| **Microarch.** | **Timer** | **B1** | Δ | **Timer** | **B1** | Δ% | **Timer** | **B1** | Δ% |
| Cortex-A72 | 7.13 | - | - | 232.41 | - | - | 4.30 | - | - |
| Cortex-A76 | 16.66 | 0.58 | -16.08 | 459.96 | 492.79 | +7.14 | 2.17 | 2.03 | -6.45 |
| Cortex-A78 | 0.91 | 0.94 | +0.03 | 617.83 | 678.59 | +9.83 | 1.62 | 1.47 | -9.26 |
| Cortex-A720 | 0.88 | 0.53 | -0.35 | 394.68 | 448.47 | +13.63 | 2.53 | 2.23 | -11.86 |
| Cortex-A725 | 6.88 | 0.04 | -6.84 | 239.71 | 188.65 | -21.30 | 4.17 | 5.30 | +27.10 |
| Cortex-X4 | 1.35 | 0.09 | -1.26 | 572.73 | 608.73 | +6.29 | 1.75 | 1.64 | -6.29 |
| Neoverse-N1 | 12.19 | 8.17 | -4.02 | 321.56 | 334.86 | +4.14 | 3.11 | 2.99 | -3.86 |
| Oryon | 19.30 | 0.51 | -18.79 | 539.98 | 741.84 | +37.38 | 1.85 | 1.35 | -27.03 |
| Kunpeng Pro | 2.79 | 3.28 | +0.49 | 305.98 | 321.76 | +5.16 | 3.27 | 3.11 | -4.89 |
| Icestorm | 0.43 | 0.43 | +0.00 | 467.51 | 487.75 | +4.33 | 2.14 | 2.05 | -4.21 |
| Firestorm | 0.61 | 0.61 | +0.00 | 605.41 | 624.82 | +3.21 | 1.65 | 1.60 | -3.03 |
| C910 | 31.99 | 0.70 | -31.29 | 57.56 | 57.35 | -0.36 | 17.37 | 17.44 | +0.40 |
| 3A5000-HV | 10.74 | 3.66 | -7.08 | 425.07 | 398.69 | -6.21 | 2.35 | 2.51 | +6.81 |

# I²SC Covert Channel

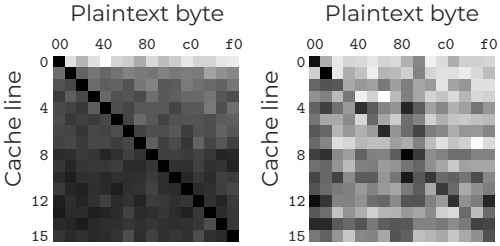
| Microarch. | Capacity (kbit s$^{-1}$, ↑) | Error Rate (%, ↓) | Throughput (kbit s$^{-1}$, ↑) | Resolution (µs, ↓) |
|---|---|---|---|---|
| Cortex-A76 | 542.02 | 0.46 | 566.11 | 1.77 |
| Cortex-A78 | 565.40 | 4.82 | 783.87 | 1.28 |
| Cortex-A720 | 544.64 | 0.01 | 545.39 | 1.83 |
| Cortex-A725 | 207.79 | 0.05 | 209.07 | 4.78 |
| Cortex-X4 | 824.14 | 0.05 | 829.67 | 1.21 |
| Neoverse-N1 | 453.30 | 0.37 | 469.93 | 2.13 |
| Oryon | 702.85 | 1.04 | 766.85 | 1.30 |
| Kunpeng Pro | 268.82 | 5.58 | 390.00 | 2.56 |
| Icestorm | 543.29 | 0.45 | 567.07 | 1.76 |
| Firestorm | 691.00 | 0.49 | 723.33 | 1.38 |
| C910 | 53.95 | 0.98 | 58.59 | 17.07 |
| 3A5000-HV | 366.05 | 1.23 | 404.90 | 2.47 |

# I²SC vs. Flush+Reload

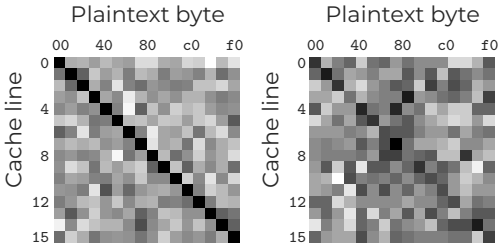
| | Capacity (kbit s$^{-1}$, ↑) | | | Error Rate (%, ↓) | | | Throughput (kbit s$^{-1}$, ↑) | | |
|---|---|---|---|---|---|---|---|---|---|
| **Microarch.** | **F+R** | **I²SC** | Δ% | **F+R** | **I²SC** | Δ | **F+R** | **I²SC** | Δ% |
| Oryon | 270.56 | 702.85 | +159.8 | 17.52 | 1.04 | -16.5 | 818.65 | 766.85 | -6.3 |
| C910 | 46.55 | 53.95 | +15.9 | 32.08 | 0.98 | -31.1 | 491.16 | 58.59 | -88.1 |
| 3A5000-HV | 213.22 | 366.05 | +71.7 | 29.97 | 1.23 | -28.7 | 1790.52 | 404.90 | -77.4 |

# AES T-Table

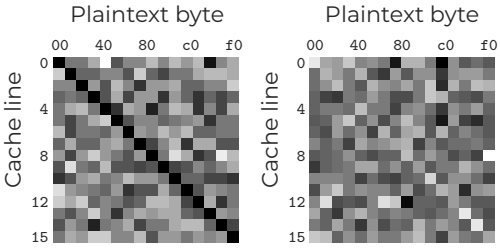
## Oryon



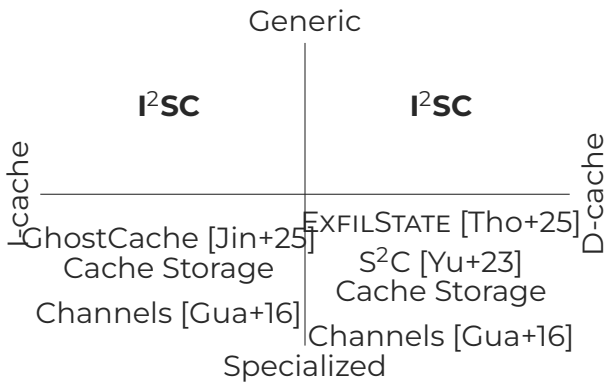

## C910




## 3A5000-HV



# Related Work



# Timer Resolution

| Microarch. | Resolution (ns) | Min inc | ΔFR (ns) | ΔFR/*min inc* | ΔiFR (ns) | ΔiFR/*min inc* |
|---|---|---|---|---|---|---|
| Cortex-A520 | 41.00 | 41.0 | 91.0 |  | 169.0 |  |
| Cortex-A72 | 119.00 | 119.0 | 166.0 |  | 135.0 |  |
| Cortex-A73 | 166.00 | 166.0 | 171.0 |  | 203.0 |  |
| Cortex-A76 | 290.99 | 291.0 | 178.0 |  | 202.0 |  |
| Cortex-A78 | 76.00 | 76.0 | 148.0 |  | 63.0 |  |
| Cortex-A720 | 40.00 | 40.0 | 83.0 |  | 72.0 |  |
| Cortex-A725 | 76.00 | 76.0 | 333.0 |  | 181.0 |  |
| Cortex-X4 | 40.00 | 40.0 | 65.0 |  | 38.0 |  |
| Neoverse-N1 | 80.00 | 80.0 | 91.0 |  | 117.0 |  |
| Oryon | 100.00 | 100.0 | 104.0 |  | 8.0 |  |
| Kunpeng Pro | 104.00 | 104.0 | 172.0 |  | 45.0 |  |
| Icestorm | 41.00 | 41.0 | 111.0 |  | 92.0 |  |
| Firestorm | 41.00 | 41.0 | 115.0 |  | 62.0 |  |
| C906 | 41.67 | 100.0 | 385.0 |  | 350.0 |  |
| C908 | 37.03 | 100.0 | 309.0 |  | 277.0 |  |
| C910 | 333.34 | 100.0 | 87.0 |  | 133.0 |  |
| X60 | 41.66 | 100.0 | 385.0 |  | 0.0 |  |
| 3A5000-HV | 20.00 | 200.0 | 1367.0 |  | 1244.0 |  |

# Used Interfaces

| Architecture | Flush (D-cache) | Flush (I-cache) | Memory Barrier | Timer |
|---|---|---|---|---|
| ARM64 | `DC CIVAC` | `IC IVAU` | `DSB ISH` | `clock_gettime`, `CLOCK_MONOTONIC` |
| RISC-V | `CBO.FLUSH` | — | `FENCE RW,RW` | `RDTIME` |
| RISC-V T-Head | `TH.DCACHE.CIVA` | `TH.ICACHE.IVA` | `FENCE rw,rw` | `RDTIME` |
| LoongArch64 (Experiments) | `CACOP 0b10011` | `CACOP 0b10000` | `DBAR 0` | `rdtime.d` |
| LoongArch64 (Eval) | L1d eviction | L1i eviction | `DBAR 0` | `RDTIME.D` |