

# From Rowhammer to GhostWrite

Advanced Exploitation and Discovery of Hardware Bugs

Fabian Thomas | HWIO Amsterdam 2024 | October 25, 2024

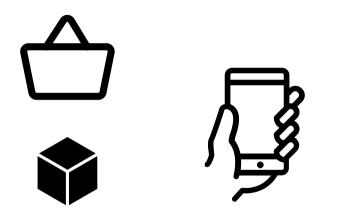


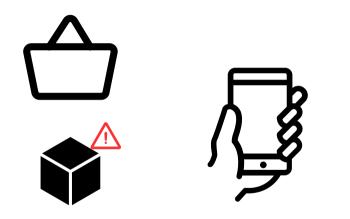


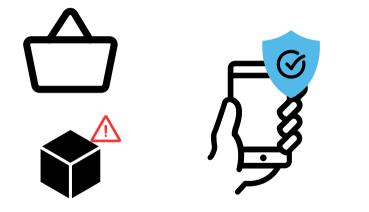


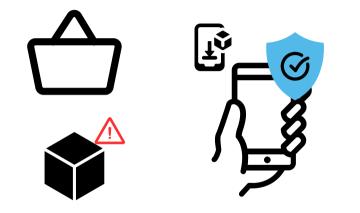








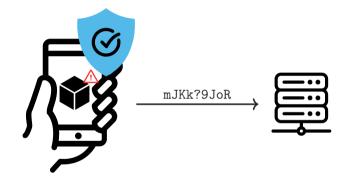
















• No permission given to app





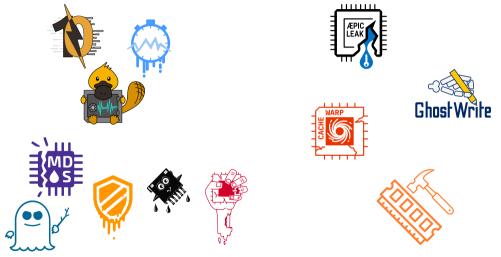
- No permission given to app
- Software security is easy: Memory-safe languages, control-flow integrity, memory tagging, ...



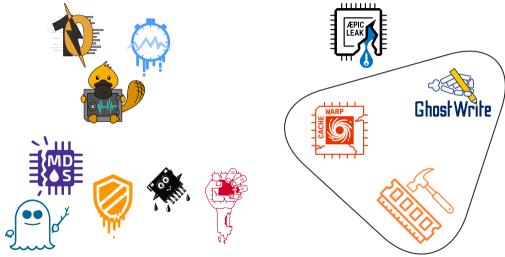


- No permission given to app
- Software security is easy: Memory-safe languages, control-flow integrity, memory tagging, ...
- Is the hardware broken?













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Twitter @fth0mas



#### **Research Group Schwarz**

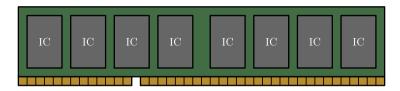


- Research focus:
  - Hardware vulnerabilities
  - $\cdot \ \ldots \ from \ software$
- · Recent discoveries:

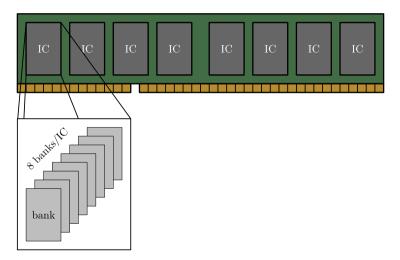




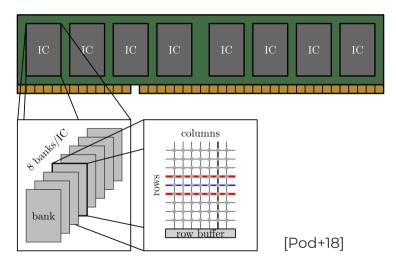






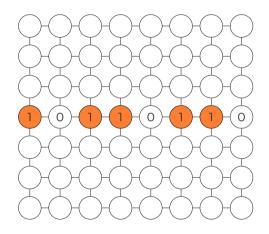






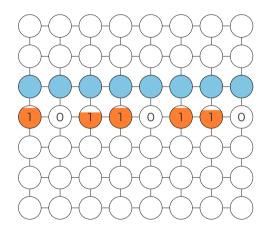


- Row activations drain
   neighbor cells
- $\cdot$  Too frequent  $\rightsquigarrow$  bit flips



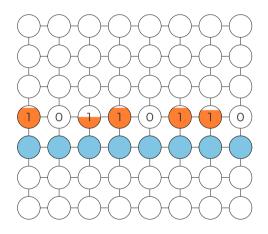


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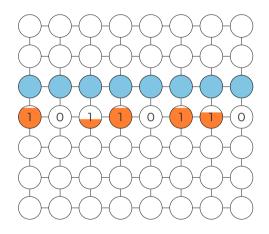


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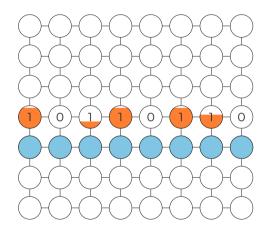


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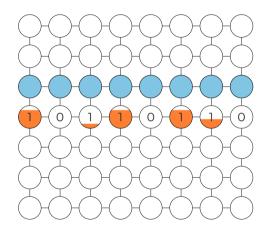


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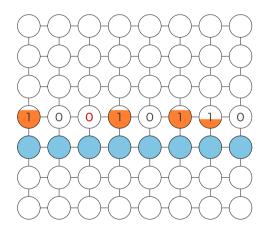


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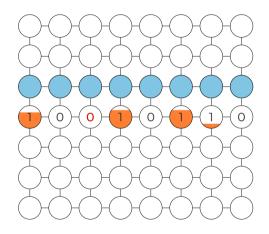


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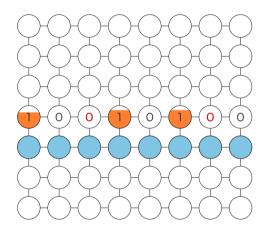


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Data Structures









Opcodes





Data Structures



Opcodes



Page Tables





Data Structures



Opcodes



Page Tables



Crypto









Secure Encrypted Virtualization





- Secure Encrypted Virtualization
- Encrypts entire VMs





- Secure Encrypted Virtualization
- Encrypts entire VMs
- Similar threat model as SGX



Flushes internal CPU caches



- Flushes internal CPU caches
- Does not write modifications to memory

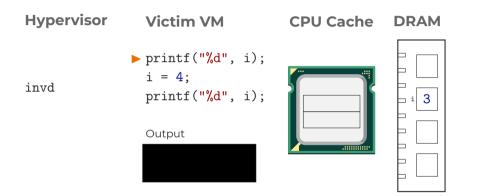


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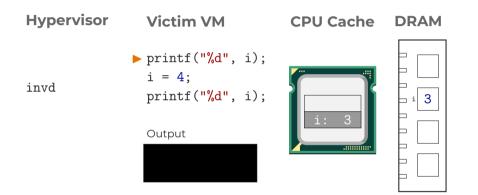
## Intel

Use this instruction with care. Data cached internally and not written back to main memory will be lost. [...] software should instead use the WBINVD instruction.

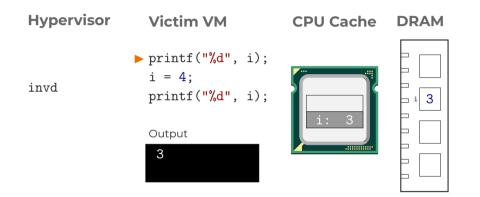




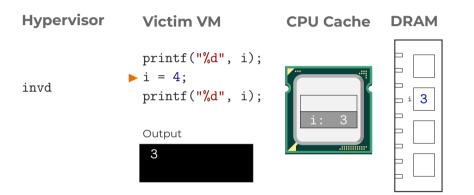




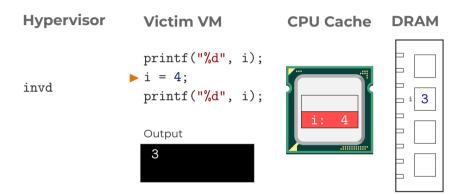




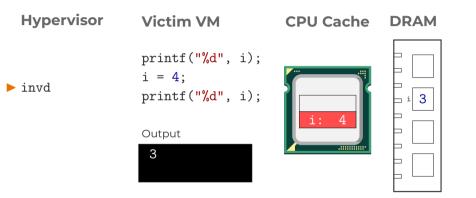




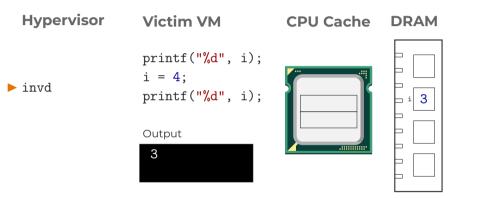




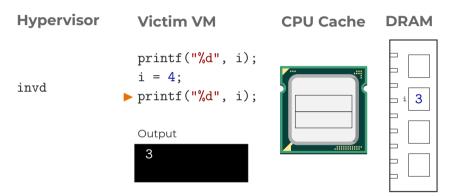




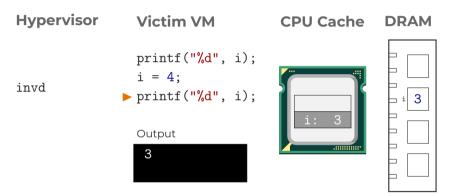




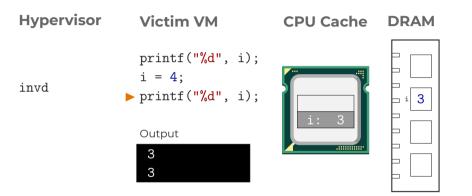














CacheWarp on sudo to gain root privileges





- CacheWarp on sudo to gain root privileges
- User ID is zero initialized





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- $\cdot\,$  sudo queries real user ID  $\rightarrow$  dropped with CacheWarp





- CacheWarp on sudo to gain root privileges
- User ID is zero initialized
- Zero = root user
- $\cdot\,$  sudo queries real user ID  $\rightarrow$  dropped with CacheWarp
- ightarrow sudo continues as root without further checks





Return addresses: implicit stores by the CPU





- Return addresses: implicit stores by the CPU
- $\cdot$  Can be reverted as well





- Return addresses: implicit stores by the CPU
- $\cdot$  Can be reverted as well
- Return uses stale value





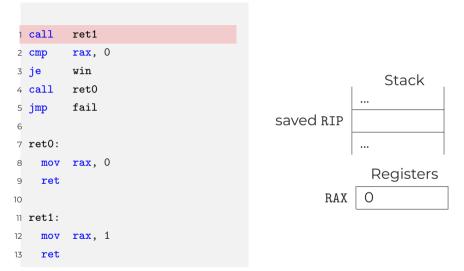
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  - $ightarrow\,$  Can be previous return address





- Return addresses: implicit stores by the CPU
- $\cdot$  Can be reverted as well
- Return uses stale value
  - ightarrow Can be previous return address
- $\rightarrow$  Jump "back in time"







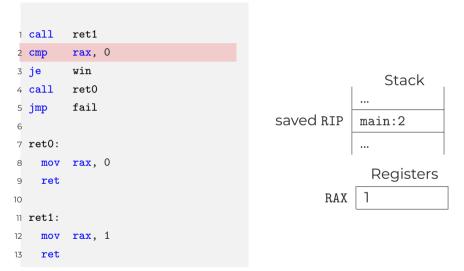






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1	call	ret1		
2	cmp	<b>rax</b> , 0		
3	je	win		Stack
4	call	ret0		
5	jmp	fail		
6	J-1		saved RIP	main:5
7	ret0:			
8	mov	<b>rax</b> , 0		
9	ret			Registers
10			RAX	1
11	ret1:			
12	mov	<b>rax</b> , 1		
13	ret			







1	call	ret1		
2	cmp	<b>rax</b> , 0		
3	je	win		Stack
4	call	ret0		SLACK
5	jmp	fail		
6			saved RIP	main:2
7	ret0:			
8	mov	<b>rax</b> , 0		
9	ret			Registers
10			RAX	0
11	ret1:			
12	mov	<b>rax</b> , 1		
13	ret			













• Timewarp on OpenSSH







- Timewarp on OpenSSH
- Login using wrong password





- Timewarp on OpenSSH
- Login using wrong password
- Timewarp to compare password hash with itself





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- $\rightarrow\,$  Entered password is not relevant





- Timewarp on OpenSSH
- Login using wrong password
- Timewarp to compare password hash with itself
- $\rightarrow\,$  Entered password is not relevant
  - Attacker is logged in via SSH





Microcode update for SEV-SNP





- Microcode update for SEV-SNP
- Converts invd to wbinvd





- Microcode update for SEV-SNP
- Converts invd to wbinvd
- $\rightarrow\,$  Modifications are written back, not dropped



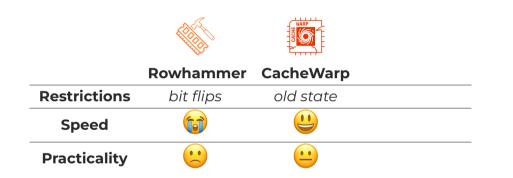


- Microcode update for SEV-SNP
- Converts invd to wbinvd
- $\rightarrow\,$  Modifications are written back, not dropped
  - Hardware fixes on Zen 4













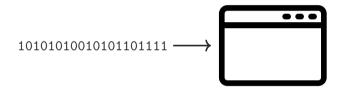






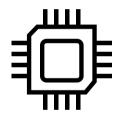












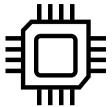


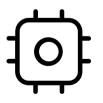




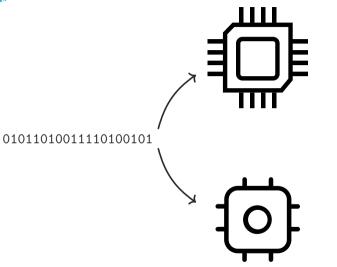




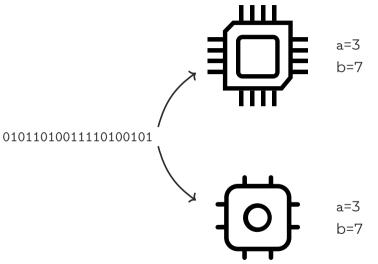




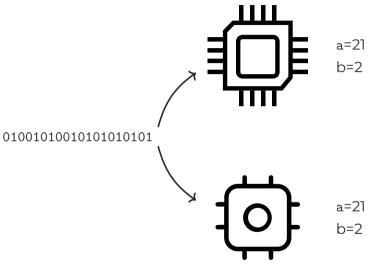




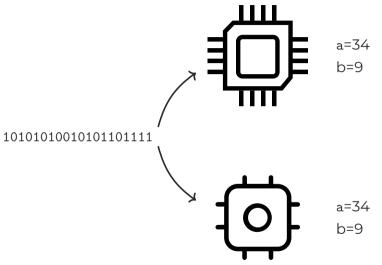




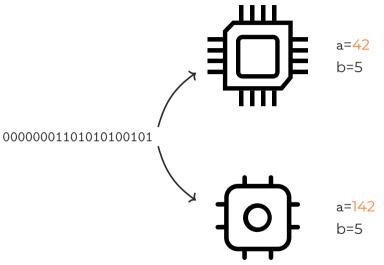


















Specifies behavior







Specifies behavior Defines legal programs









Specifies behavior Defines legal programs



Licensing fees











open, community-driven









open, community-driven no licensing fees









open, community-driven no licensing fees



well designed









open, community-driven no licensing fees

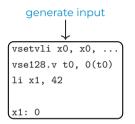




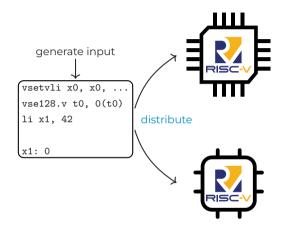
well designed

extensible

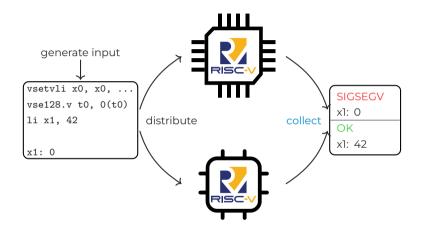




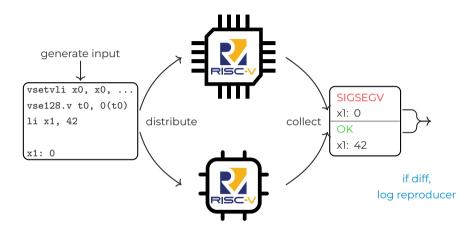




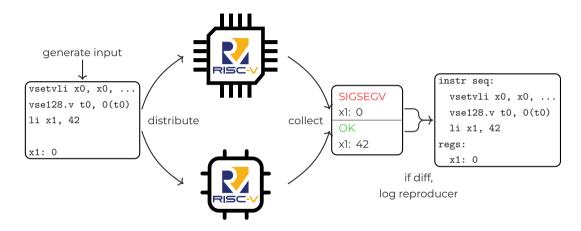








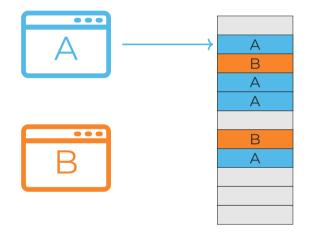




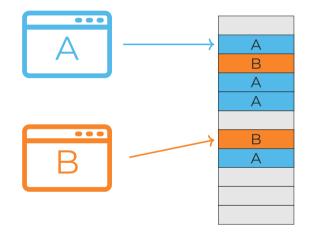




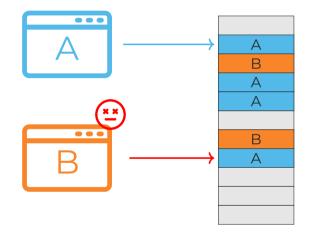




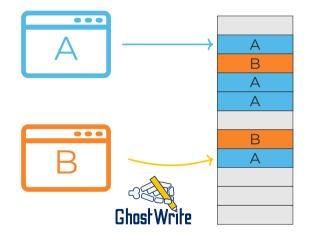














## Software World





## Software World

## Hardware World



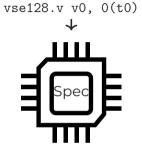


mv t0, addr vmv.v.x v0, value vsetvli zero, zero, e8, m1 vse128.v v0, 0(t0)



mv t0, addr
vmv.v.x v0, value
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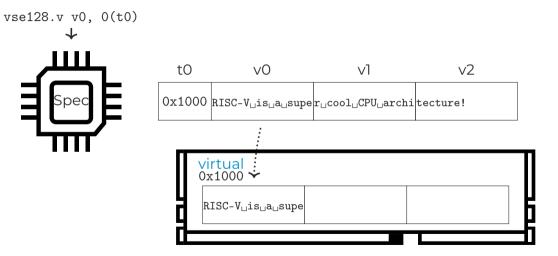




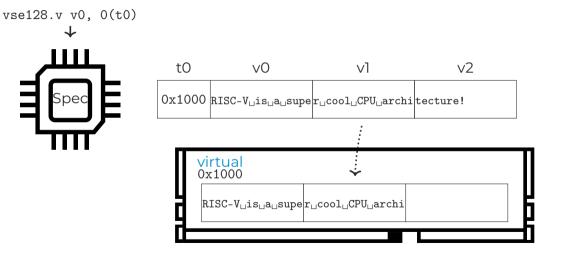
tO	VO	$\lor$ 1	v2
0x1000	$RISC-V_{\sqcup}is_{\sqcup}a_{\sqcup}supe$	r <sub>u</sub> cool <sub>u</sub> CPU <sub>u</sub> archi	tecture!



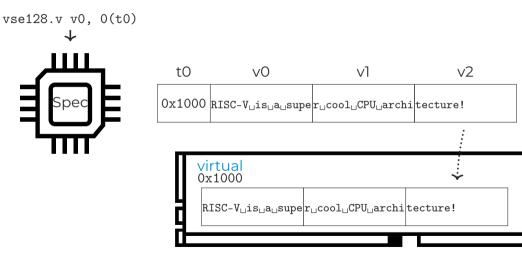




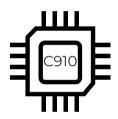


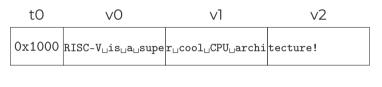


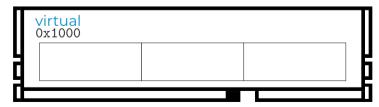




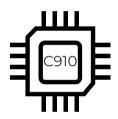








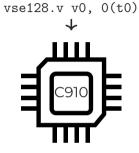




tO	VO	$\lor$ 1	v2
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ſ	virtual <sub>0x1000</sub>				
	hardwea	ar.io <sub>u</sub> is <sub>u</sub> a	$_{\sqcup} \texttt{super}_{\sqcup} \texttt{cool}_{\sqcup} \texttt{hard}$	ware_conference!	H
C					

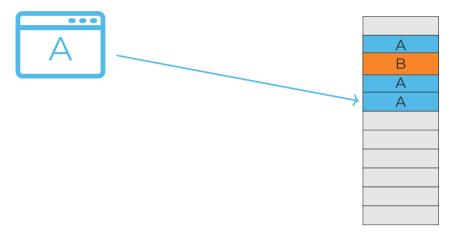




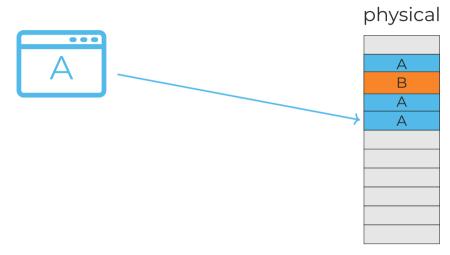
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	$hardwear.io_{ls_{la}}$	H
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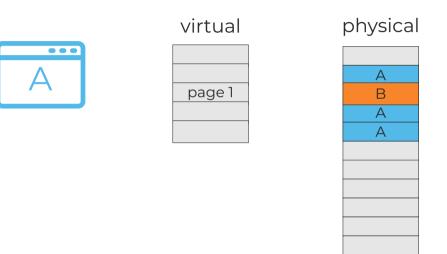




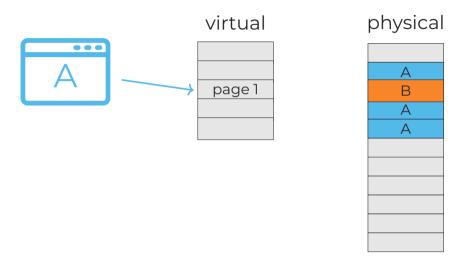




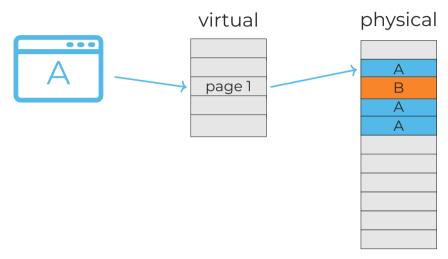




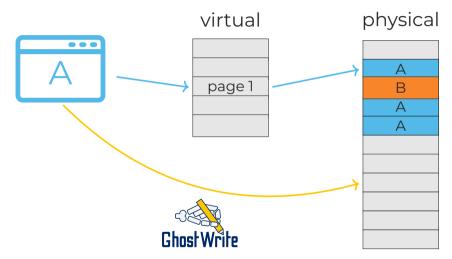




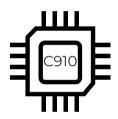








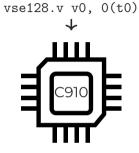




tO	VO	V٦	v2
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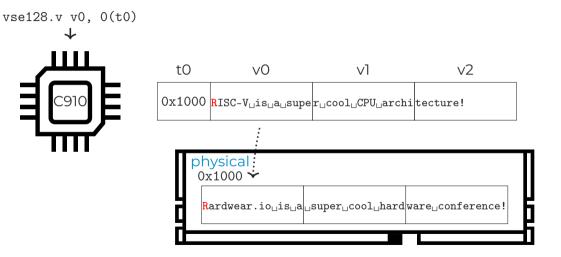




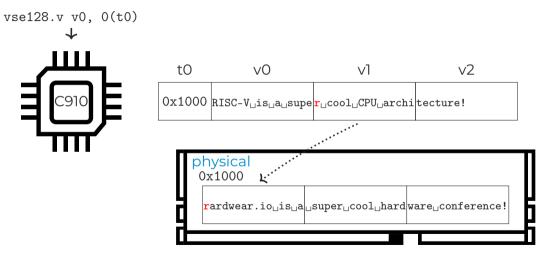
tO	VO		v2
0x1000	RISC-V <sub>u</sub> is <sub>u</sub> ausupe	r <sub>u</sub> cool <sub>u</sub> CPU <sub>u</sub> archi	tecture!

	physical 0x1000			Τ
	tardwear.io⊔is⊔a	$_{\sqcup} \texttt{super}_{\sqcup} \texttt{cool}_{\sqcup} \texttt{hard}$	ware_conference!	H
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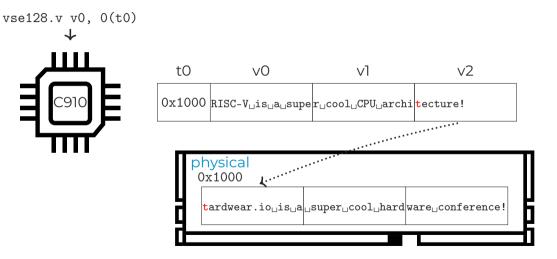
















• One of the fastest RISC-V CPUs





- One of the fastest RISC-V CPUs
- 4 cores, 2GHz, vector extension





- One of the fastest RISC-V CPUs
- 4 cores, 2GHz, vector extension
- · Available in the cloud



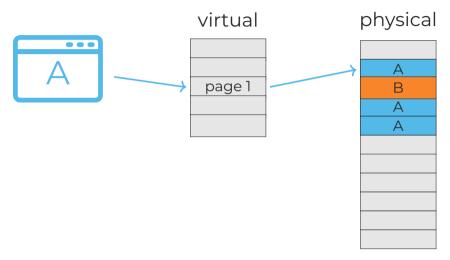




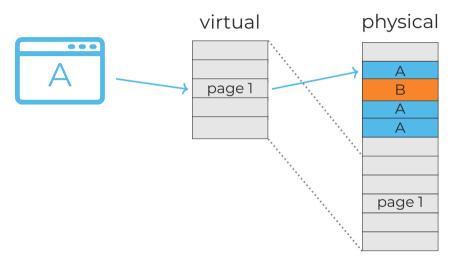
- One of the fastest RISC-V CPUs
- 4 cores, 2GHz, vector extension
- Available in the cloud
- ... and laptops



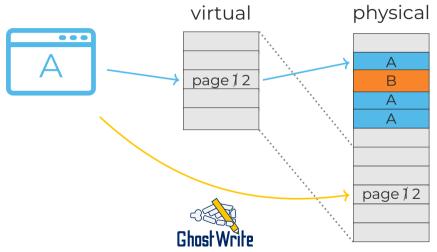




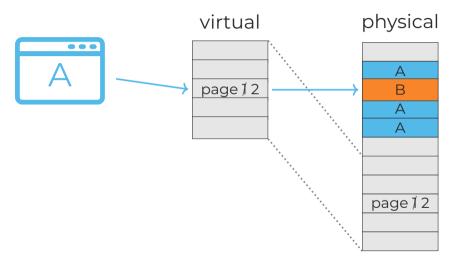




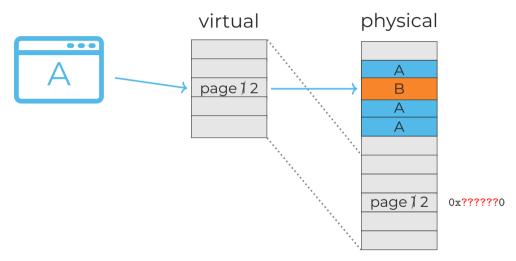










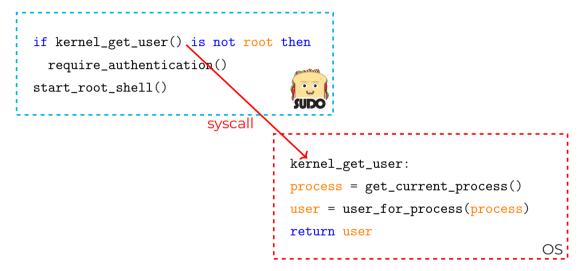




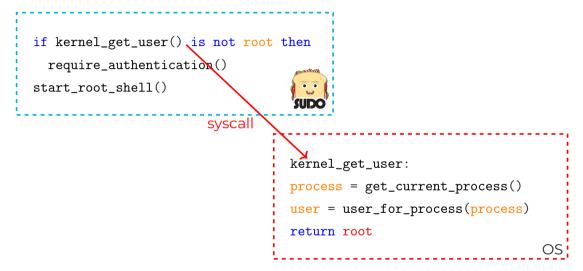
```
if kernel_get_user() is not root then
  require_authentication()
start_root_shell()
```

```
kernel_get_user:
process = get_current_process()
user = user_for_process(process)
return user
OS
```

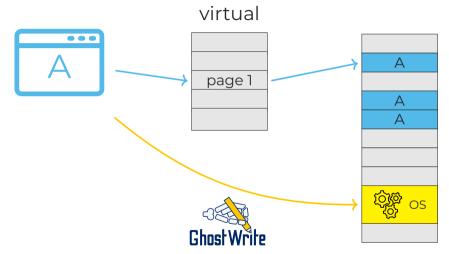
















• C910 has no microcode







- C910 has no microcode
- OS mitigation: disable vector extension





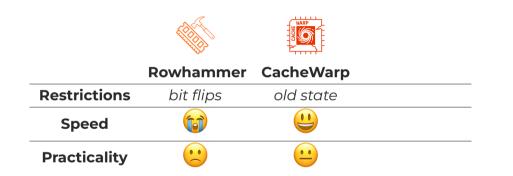
- C910 has no microcode
- · OS mitigation: disable vector extension
- Up to 33% overhead



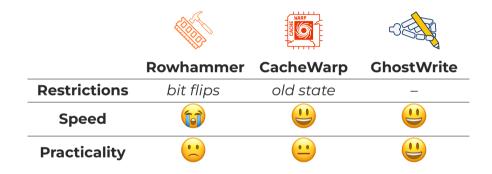


- C910 has no microcode
- · OS mitigation: disable vector extension
- Up to 33% overhead
- + Lose  $\sim 50\%$  instructions

































We can't trust system if hardware broken













We can't trust system if hardware broken



Quality control important











We can't trust system if hardware broken



-36 Ghost Write

Quality control important

Remedy: Configurable hardware











@fthOmas fabianthomas.de

Lots of hardware bugs

We can't trust system if hardware broken



Quality control important

Remedy: Configurable hardware



## References

## [Pod+18] D. Poddebniak, J. Somorovsky, S. Schinzel, M. Lochter, and P. Rösler. Attacking deterministic signature schemes using fault attacks. In: EuroS&P). 2018.











OS: disable extension





OS: disable extension

up to 33% overhead lose  $\sim$  50% instructions



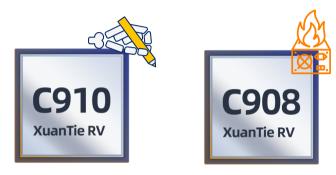


OS: disable extension

up to 33% overhead

lose  $\sim 50\%$  instructions





OS: disable extension up to 33% overhead lose  $\sim$  50% instructions

OS: disable extension





OS: disable extensionOS: disable extensionup to 33% overheadup to 77% overheadlose ~ 50% instructionslose ~ 50% instructions







OS: disable extension OS: disable extension up to 33% overhead up to 77% overhead lose  $\sim$  50% instructions lose  $\sim$  50% instructions







OS<sup>1</sup> disable extension OS<sup>•</sup> disable extension up to 33% overhead lose  $\sim$  50% instructions lose  $\sim$  50% instructions

up to 77% overhead

no mitigation



